Philips Components–Signetics

Document No.	853-0153
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
Memory Products	

82S09
82S09A
576-bit TTL bipolar RAM

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/09A features Open-Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

Ordering codes are listed in the Ordering Information Table.

The 82S09 and 82S09A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

FEATURES

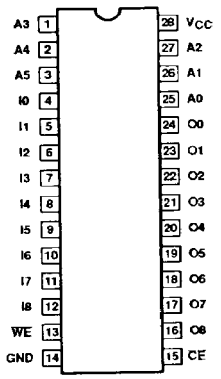
- Address access time:
  - N82S09: 45ns max
  - N82S09A: 35ns max
- Write cycle time:
  - N82S09/09A: 45ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100μA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- Output is non-blanked during Write
- One Chip Enable input
- Outputs: Open-Collector

APPLICATIONS

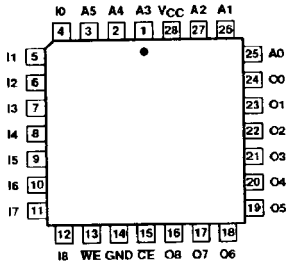
- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATIONS

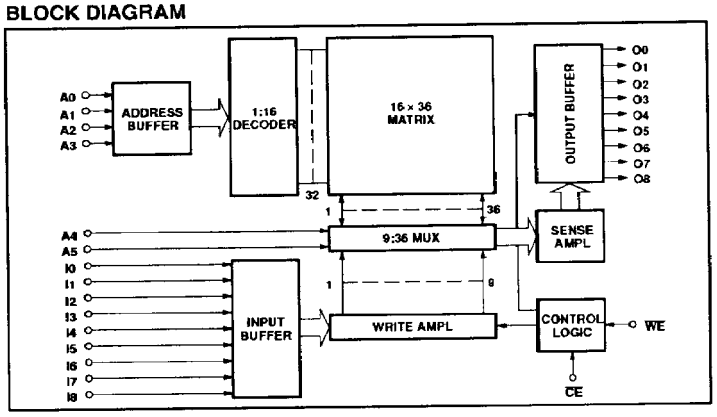
N Package



A Package



BLOCK DIAGRAM



576-bit TTL bipolar RAM (64 × 9) — 82S09 / 82S09A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Plastic Dual-In-Line 600mil-wide	N82S09 N, N82S09A N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S09 A, N82S09A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input voltage[1]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[2]	V_{CC} = 4.75V, I_{IN} = –12mA			–1.5	V
Output voltage[1]						
V_{OL}	Low[3]	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			–100	µA
I_{IH}	High	V_{IN} = 5.5V			25	µA
Output current						
I_{OLK}	Leakage[4]	V_{CC} = 5.25V, V_{OUT} = 5.5V			40	µA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V			190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. All voltage values are with respect to network ground.
2. Test each input one at a time
3. Measured with the logic Low stored.Output sink current is applied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the Write Enable and Chip Enable inputs grounded, all other inputs at 0.45V, and the outputs open.
6. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	O_N
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disable	1	X	X	1

X = Don't care

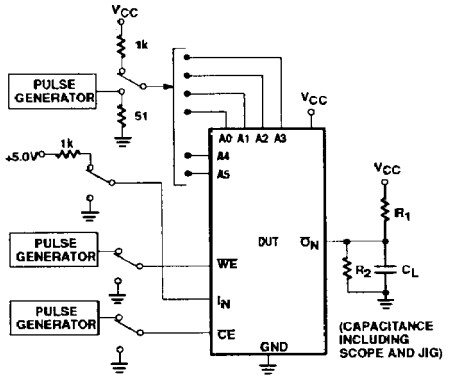
AC ELECTRICAL CHARACTERISTICS

$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S09			N82S09A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Access time										
t_{AA}	Address	Output	Address			45			35	ns
t_{CE}	Chip Enable	Output	Output			30			25	ns
Disable time[1]										
t_{CD}		Output	Chip Enable			30			25	ns
t_{WA}	Valid time	Output	Write Enable			30			25	ns
Setup and hold time										
t_{WSA}[2]	Setup time	Write Enable	Address	5			5			ns
t_{WHA}	Hold time	Write Enable	Address	5			5			ns
t_{WSD}	Setup time	Write Enable	Data in	35			30			ns
t_{WHD}	Hold time	Write Enable	Data in	5			5			ns
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	5			5			ns
t_{WHC}	Hold time	Write Enable	$\overline{CE}$	5			5			ns
Pulse width[3]										
t_{WP}[4]	Write Enable			35			35			ns

NOTES:
1. Measured at a delta of 0.5V from Logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
2. Measured with minimum t_{WP}.
3. Minimum required to gurarantee a Write into the slowest bit.
4. Measured with minimum t_{WSA}.
5. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

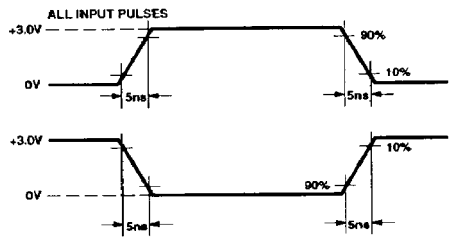
TEST LOAD CIRCUIT



All resistor's values are typical and in ohms.

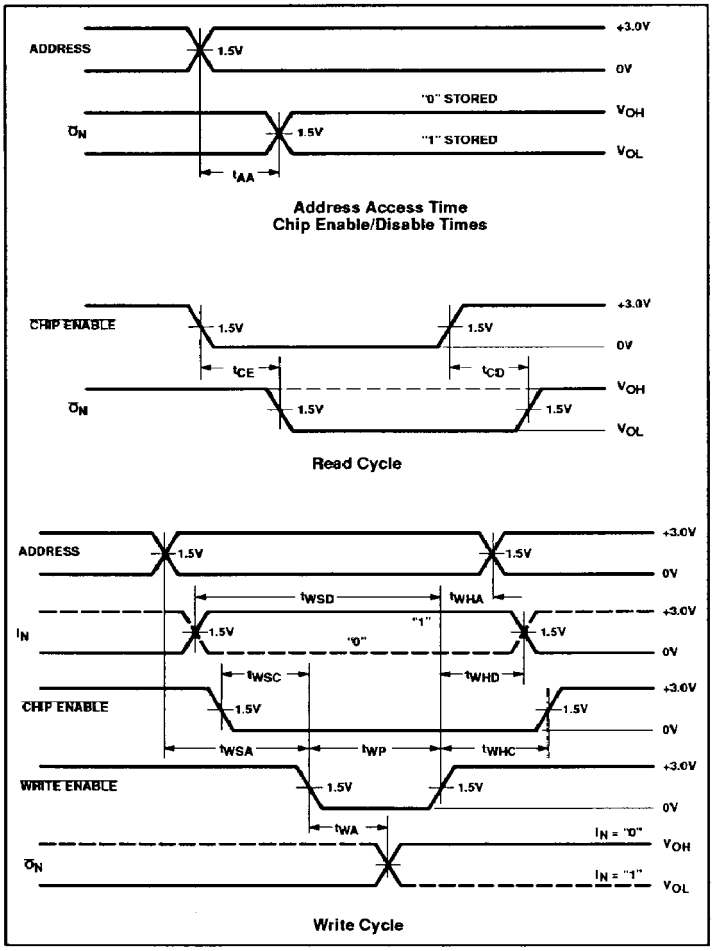
Loading Conditions

VOLTAGE WAVEFORMS



Input Pulses

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-State.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)
t_{WA}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.