82S09-I,N

DESCRIPTION

The organization of this device allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature ranges. (0°C to +75°C) specify N82S09, and for the military temperature range (-55°C to +125°C) specify S82S09.

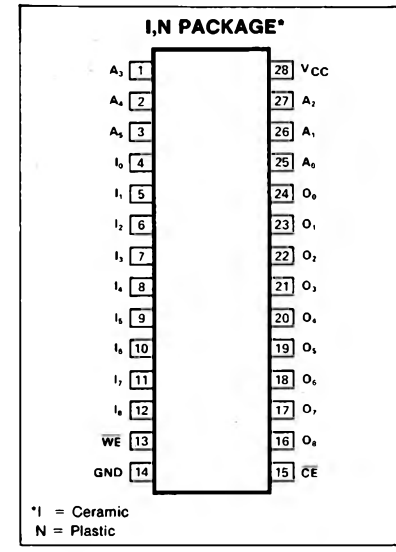
FEATURES

- **Address access time:**
  N82S09: 45ns max
  S82S09: 80ns max
- **Write cycle time:**
  N82S09: 45ns max
  S82S09: 75ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S09: -100μA max
  S82S09: -150μA max
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



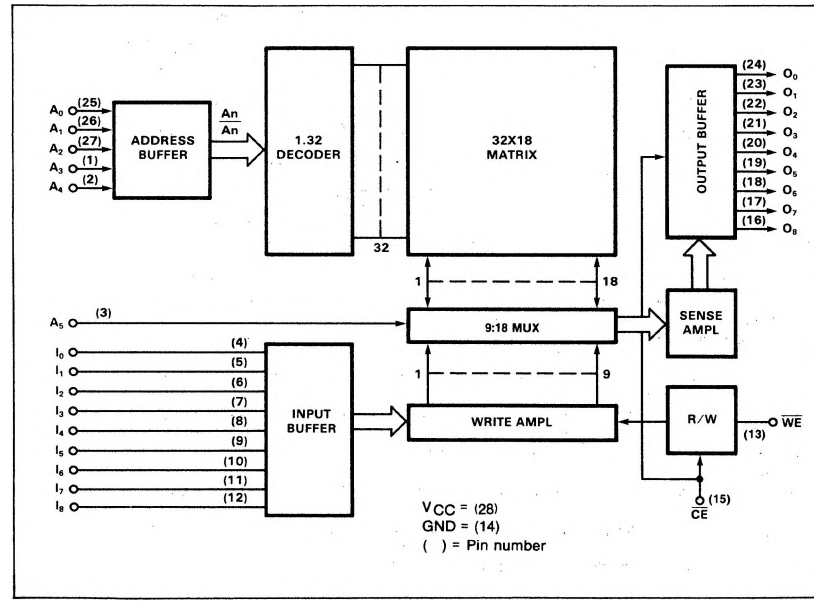
*I = Ceramic
N = Plastic

TRUTH TABLE

MODE	CE	WE	I_N	O_N
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10)	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09	0 to +75	
	S82S09	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[1]

N82S09: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S09: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITONS	N82S09			S82S09			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage								V
V_{OL}	Low[4]	V_{CC} = Min, I_{OL} = 6.4mA		0.35	0.5		0.35	0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current								μA
I_{OLK}	Leakage[5]	V_{CC} = Max, V_{OUT} = 5.5V		1	40		1	60	
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	190		150	200	mA
	Capacitance	V_{CC} =5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

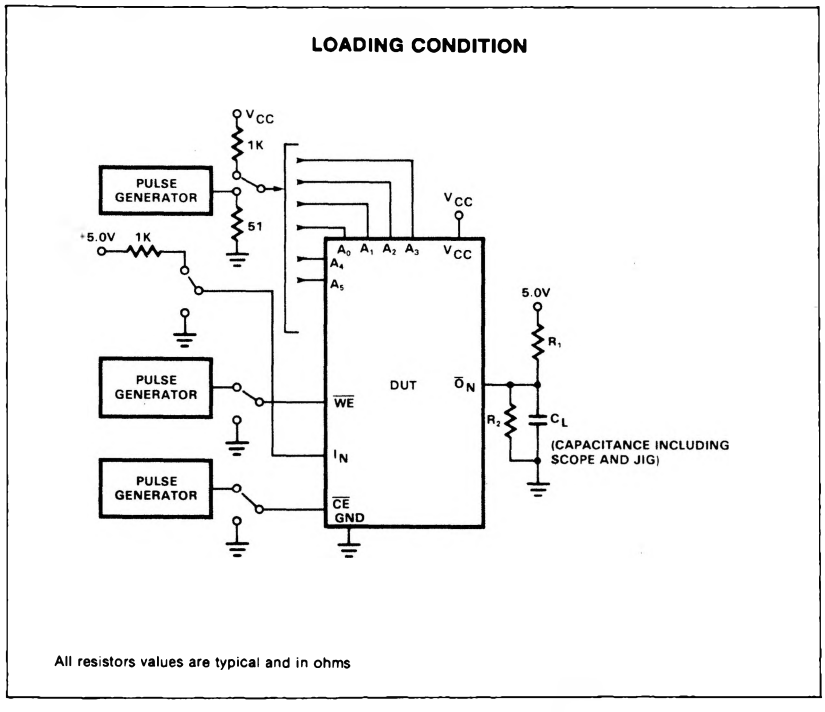
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, See ac test load
N82S09: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S09: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S09			S82S09			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}	Address				30	45		30	80	
T_{CE}	Chip enable				15	30		15	50	
T_{CD}	Disable time	Output	Chip enable		15	30		15	50	ns
T_{WD}	Valid time	Output	Write enable		25	50		25	80	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5	0		10	0		
T_{WHA}	Hold time									
T_{WSD}	Setup time	Write enable	Data in	35	25		50	25		
T_{WHD}	Hold time			5	0		5	0		
T_{WSC}	Setup time	Write enable	CE	5	0		10	0		
T_{WHC}	Hold time									
	Pulse width									ns
T_{WP}	Write enable			35	25		50	25		

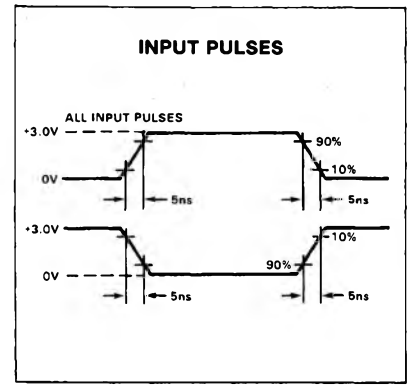
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE}$.
6. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
7. Minimum required to guarantee a Write into the slowest bit.
8. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT

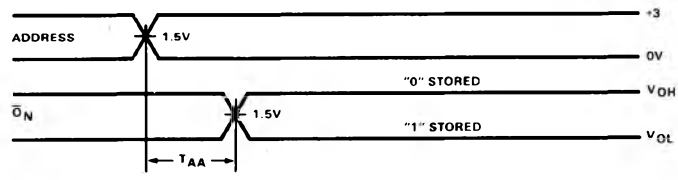


VOLTAGE WAVEFORM

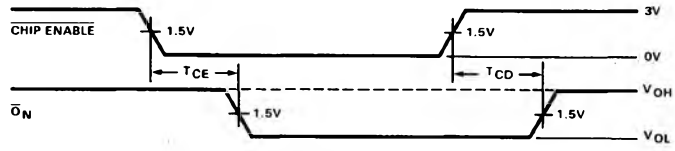


TIMING DIAGRAMS

READ CYCLE

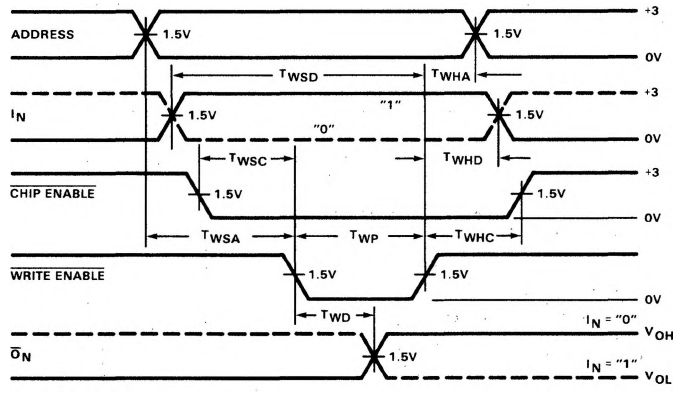


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.