PRESETTABLE LOW POWER DECADE/BINARY COUNTER

8292
8293

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state, A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.
The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

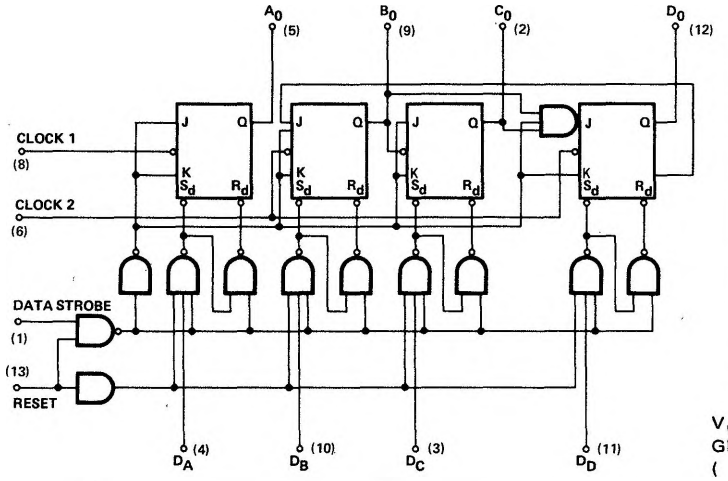
The various counter arrangements, as well as additional applications suggestions may be found in the Signetics handbook "DESIGNING WITH MSI," Counters and Shift Registers, Volumn I.

LOGIC DIAGRAMS AND TRUTH TABLES

8292

Bi-Quinary (5-2)

Input	B_0	C_0	D_0	A_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	1



Decade (BCD)

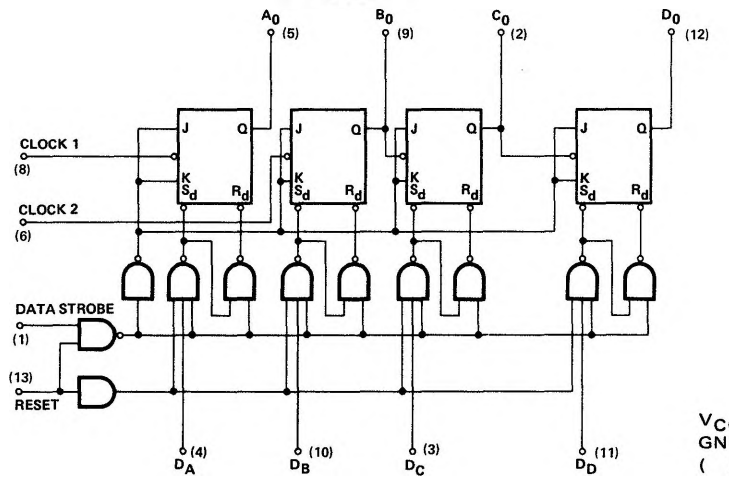
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

8293

Binary

Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V		A_{OUT}	-100μA	6,8
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V		A_{OUT}	3.2mA	6,9
"0" Input Current											
Data Strobe	-0.1		-0.4	mA	0.4V		5.25V				
Data Inputs	-0.1		-0.4	mA		0.4V					
Reset	-0.1		-0.6	mA	5.25V		0.4V				
Clock 1	-0.1		-0.6	mA	5.25V			0.4V			
Clock 2 (8292)	-0.1		-1.2	mA	5.25V				0.4V		
Clock 2 (8293)	-0.1		-0.6	mA	5.25V				0.4V		
"1" Input Current											
Data Strobe			20	μA	4.5V		0.0V				
Data Inputs			20	μA		4.5V					
Reset			40	μA	0.0V		4.5V				
Clock 1			40	μA	0.0V			4.5V			
Clock 2 (8292)			80	μA	0.0V				4.5V		
Clock 2 (8293)			40	μA	0.0V				4.5V		
Output Short Circuit Current	-5		-45	mA	0.0V					0.0V	7
Input Voltage Rating											
Data Strobe					10mA						
Clock 1 and 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				

$T_A = 25°C$ and $V_{CC} = 5.0V$

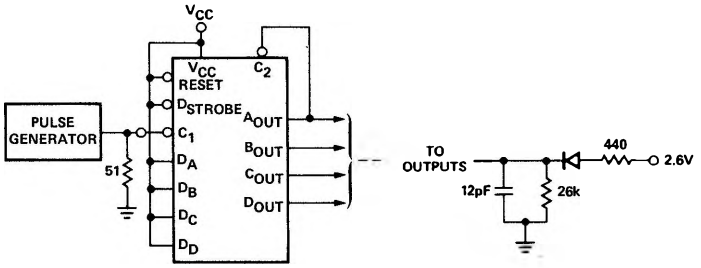
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Power/Current Consumption		52.5/ 10	69/ 13.1	mw/ mA			0.0V	0.0V	0.0V		13
Clock Mode t_{on} Delay (All Bits)		37	55	ns							10
Clock Mode t_{off} Delay (All Bits)		32	55	ns							10
Strobed Data t_{on} Delay (All Bits)		80	100	ns							10
Strobed Data t_{off} Delay (All Bits)		80	100	ns							10
Clock Mode Switching Test			75	ns							12
Strobe Pulse Width		60	75	ns		0.8V	2.0V	2.0V	A_{OUT}		
Reset Pulse Width		45	60	ns		2.0V	2.0V	2.0V	A_{OUT}		
Strobe/Reset Release Time		80		ns					A_{OUT}		
Toggle Rate	5	10		MHz							

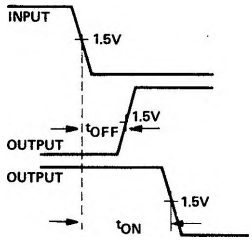
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Not more than one output should be shorted at a time.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Refer to AC Test Figure.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. This test guarantees the device will reliably trigger on a pulse with a 75ns fall-time or less.
13. V_{CC} = 5.25 volts.

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY

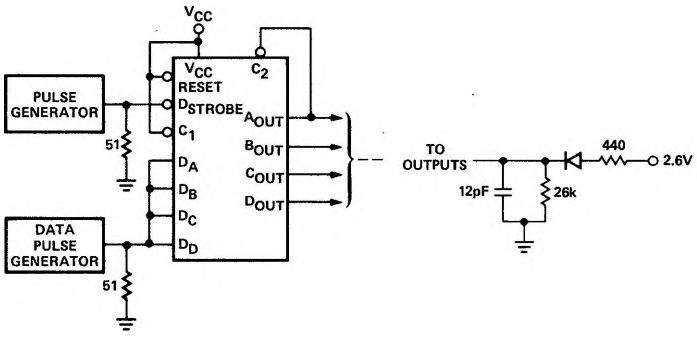


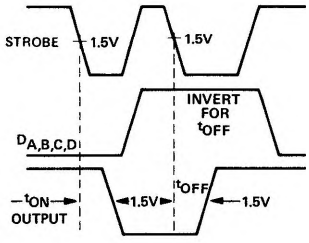


INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

NOTE:
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

STROBED DATA t_{on}/t_{off} DELAY



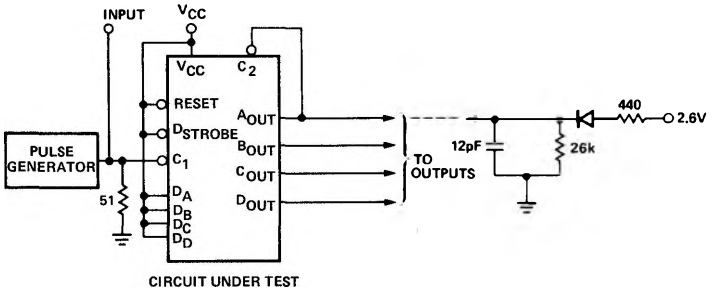


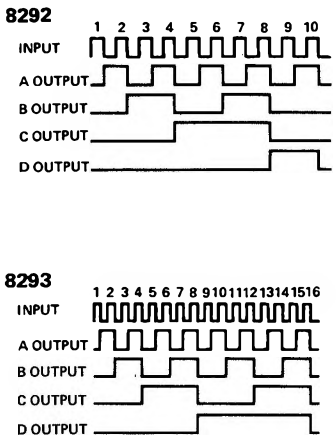
Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$

Data,
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f = 5ns$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

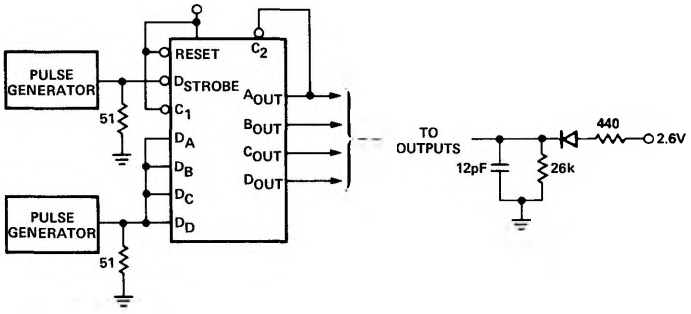
CLOCK MODE SWITCHING TEST

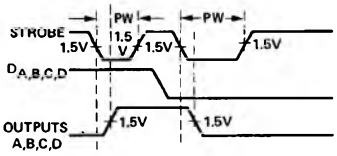




INPUT PULSE:
Amplitude = 3.4V
P.W. = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns
t_f = 75ns

MINIMUM STROBE PULSE WIDTH

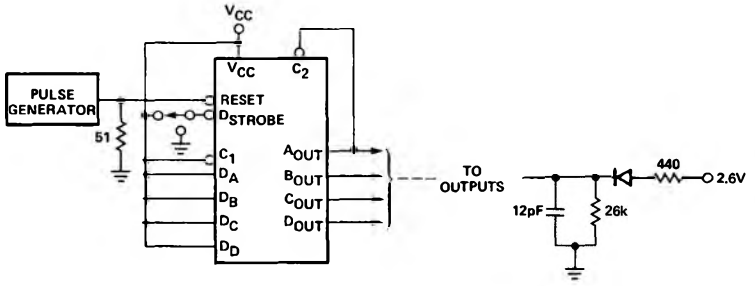


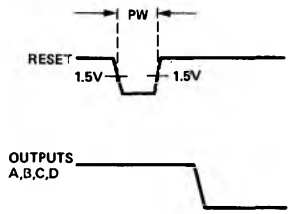


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

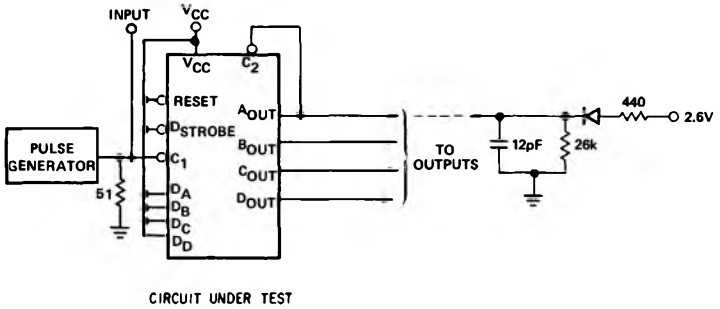
MINIMUM RESET PULSE WIDTH



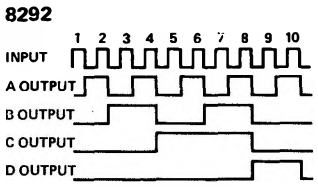


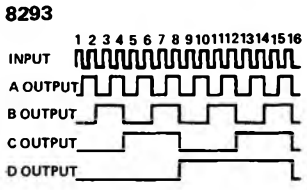
INPUT PULSE:
Amplitude 2.6V
$t_r = t_f$ = 5ns max.
NOTE: Outputs must be previously brought high by placing a "Q" on the D strobe input. A pulse generator may be substituted for the switch.

TOGGLE RATE



CIRCUIT UNDER TEST

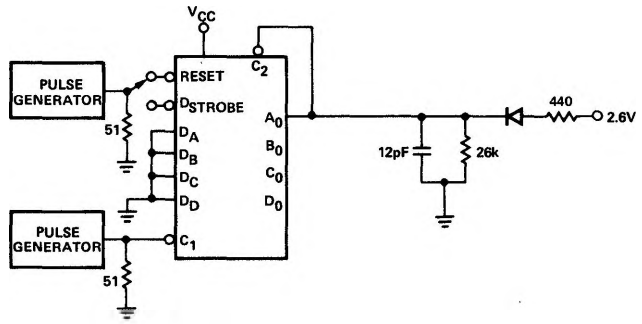


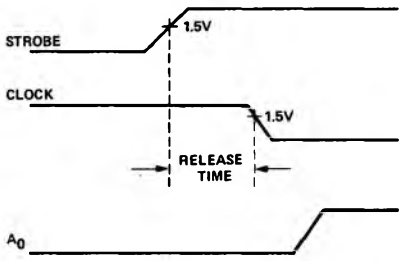


INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

STROBE/RESET RELEASE TIME





CLOCK, STROBE/RESET:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1MHz, V_{ac} = 25mV_{rms}.
3. All diodes are 1N916.