

PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER

8290 8291

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1"

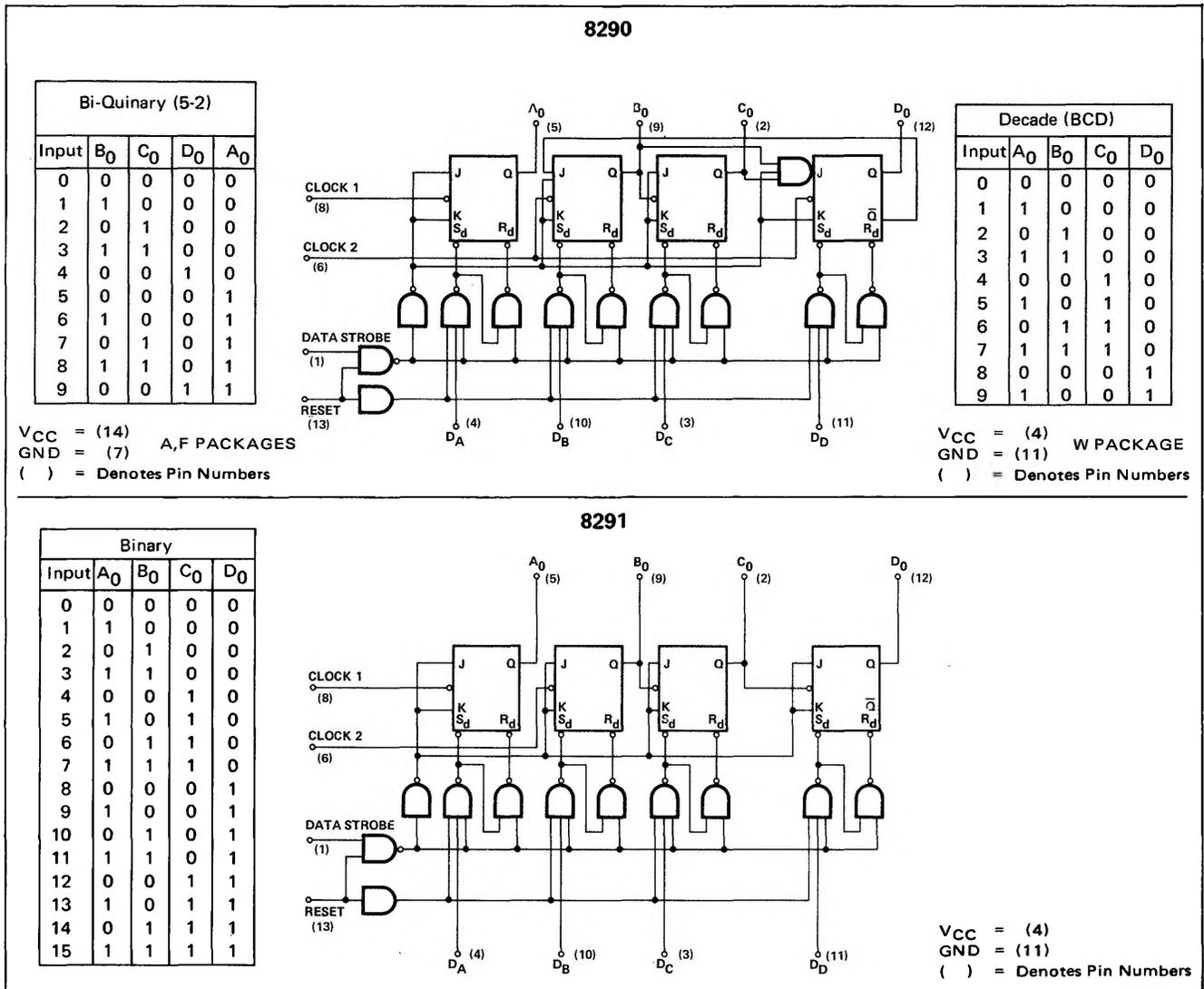
or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

The various counter arrangements, as well as additional applications suggestions may be found in the Signetics Handbook "DESIGNING WITH MSI—Counters and Shift Registers Vol. 1.

LOGIC DIAGRAMS AND TRUTH TABLES



SIGNETICS DIGITAL 8000 SERIES TTL/MSI – 8290/91

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES	
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS		
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V				-200µA	6, 8
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V				9.6mA	6, 9
"0" Input Current												
Data Strobe	-0.1		-1.6	mA	0.4		5.25V					
Data Inputs	-0.1		-1.2	mA		0.4						
Reset	-0.1		-2.8	mA	5.25V		0.4					
Clock 1	-0.1		-4.8	mA	5.25V			0.4				
Clock 2 (8290)	-0.1		-4.8	mA	5.25V				0.4			
Clock 2 (8291)	-0.1		-2.4	mA	5.25V				0.4			
"1" Input Current												
Data Strobe			40	µA	4.5V		0.0V					
Data Inputs			40	µA		4.5V						
Reset			80	µA	0.0V		4.5V					
Clock 1			80	µA	0.0V			4.5V				
Clock 2 (8290)			120	µA	0.0V				4.5V			
Clock 2 (8291)			80	µA	0.0V				4.5V			
Output Short Circuit Current A	-20		-70	mA							0.0V	13
B, C, D	-10		-60	mA							0.0V	13
Input Voltage Rating												
Data Strobe	5.5			V	10mA							
Clock 1 & 2	5.5			V				10mA	10mA			
Data Inputs	5.5			V		10mA						
Reset	5.5			V			10mA					

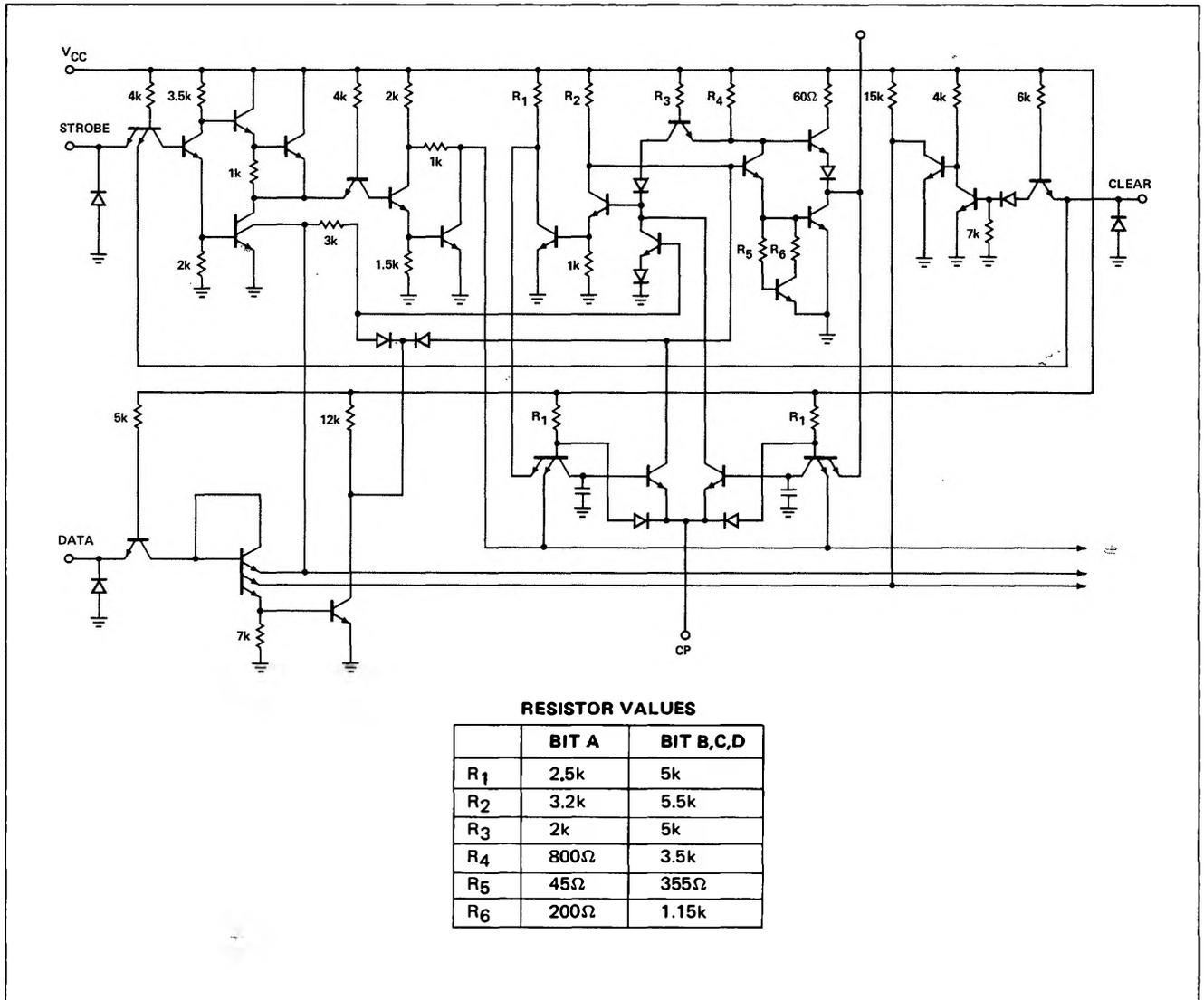
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES	
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS		
Power Consumption/ Supply Current		190/ 36.5	255/ 48.5	mW/ mA			0.0V	0.0V	0.0V			13
Strobe Pulse Width		15		ns						A _{OUT}		9
Reset Pulse Width		25		ns						A _{OUT}		9
Strobe/Reset Release Time		20		ns						A _{OUT}		9
Clock Mode t _{on} Delay												
Bit A		12	25	ns								9
Bits B, C, D		15	30	ns								9
Clock Mode t _{off} Delay												
Bit A		12	23	ns								9
Bits B, C, D		15	25	ns								9
Strobed Data t _{on} Delay (All Bits)		31	42	ns								9
Strobed Data t _{off} Delay (All Bits)		33	42	ns								9
Toggle Rate	40	60		MHz								9
Clock Mode Switching Test			75	ns								9, 11

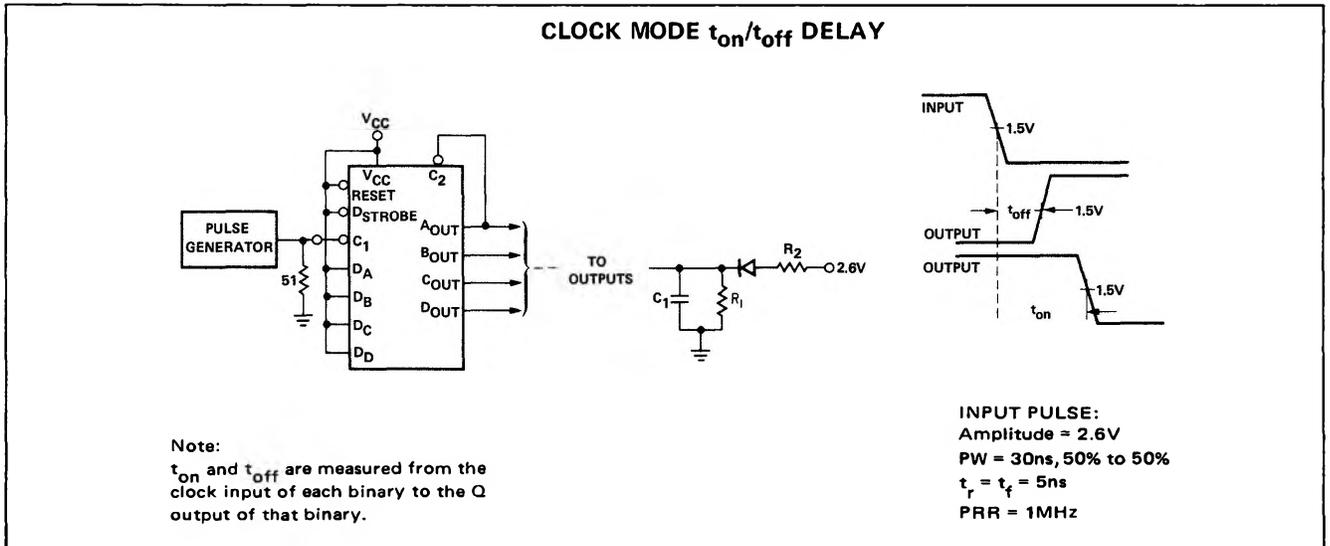
NOTES:

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND Logic definition:
"UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each output and the associated data input independently.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC}.
- Refer to AC Test Figures.
- Manufacturer reserves the right to make design and process changes and improvements.
- This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.
- Not more than one output should be shorted at a time.
- V_{CC} = 5.25V.

SCHEMATIC DIAGRAM

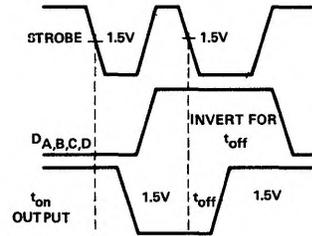
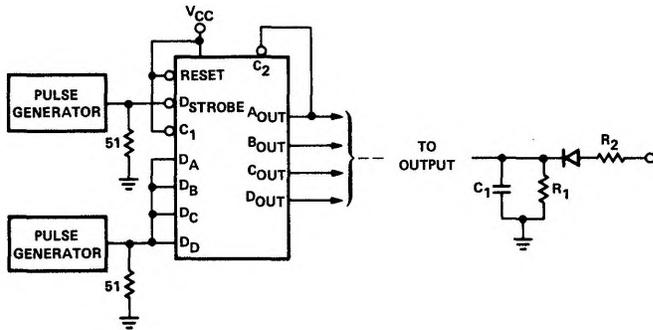


AC TEST FIGURES AND WAVEFORMS



AC TEST FIGURES AND WAVEFORMS (Cont'd)

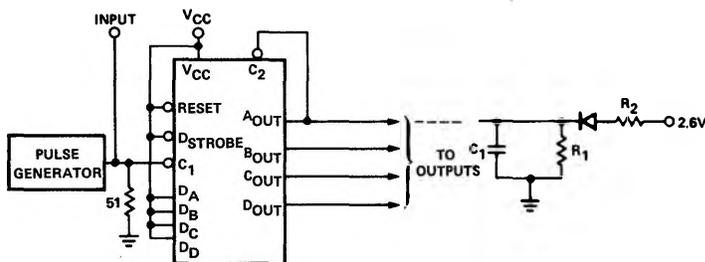
STROBED DATA t_{on}/t_{off} DELAY



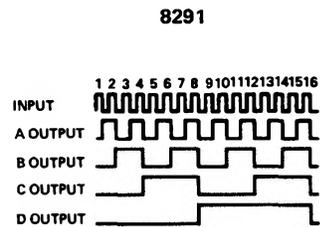
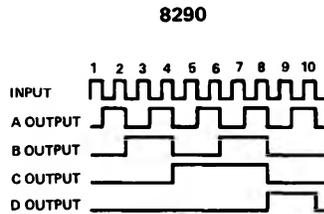
STROBE, PA = 2.6V
 PW = 300ns, 50% to 50%
 PRR = 1MHz
 $t_r = t_f = 5ns$

DATA, PA = 2.6V
 PW = 500ns, 50% to 50%
 PRR = 500kHz
 $t_r = t_f = 5ns$

CLOCK MODE SWITCHING TEST

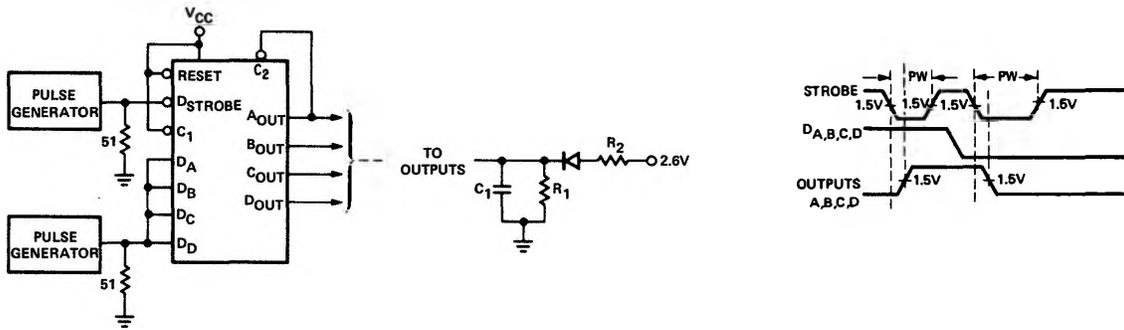


INPUT PULSE:
 Amplitude = 3.4V
 PW = 100ns, 50% to 50%
 PRR = 2.5MHz
 $t_r = 20ns, t_f = 75ns$



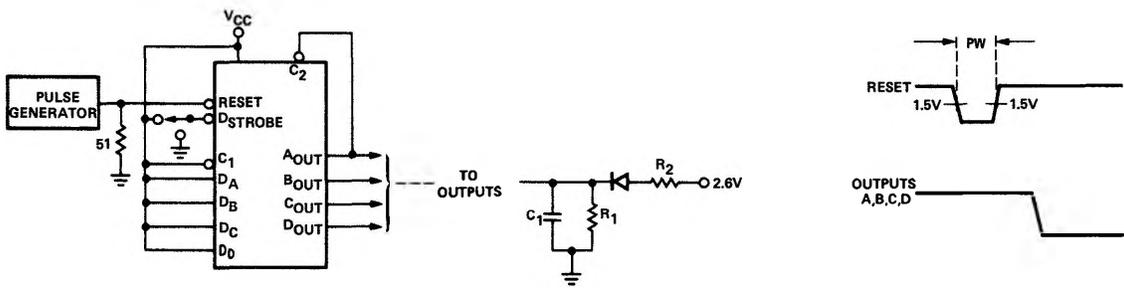
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM STROBE PULSE WIDTH



INPUT PULSE:
 Amplitude = 2.6V
 $t_r = t_f = 5\text{ns}$

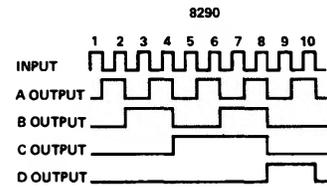
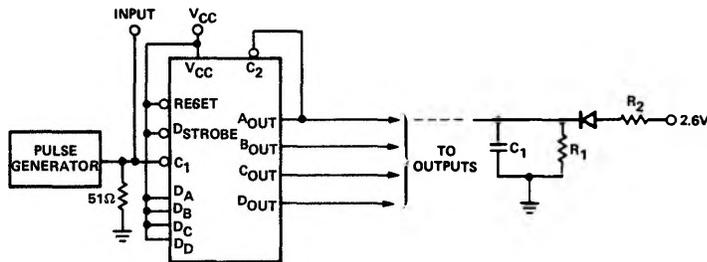
MINIMUM RESET PULSE WIDTH



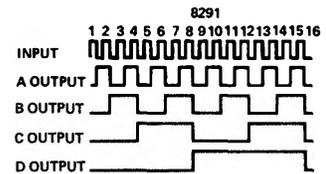
INPUT PULSE:
 Amplitude = 2.6V
 $t_r = t_f = 5\text{ns}$.
 Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

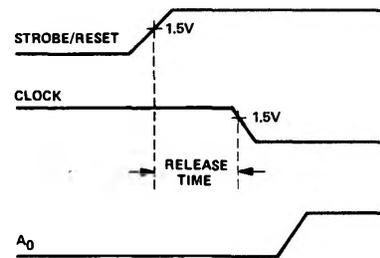
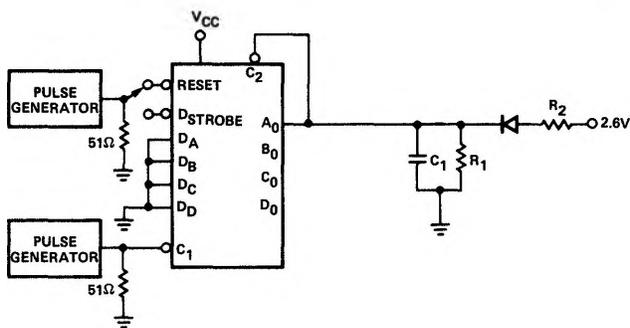
TOGGLE RATE



INPUT PULSE:
 Amplitude = 2.6V
 $t_r = t_f = 5\text{ns max.}$
 PRR = 40MHz, 50% duty cycle.



STROBE/RESET RELEASE TIME



NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{ac} = 25\text{mV}_{rms}$.
3. All diodes are 1N916.
4. $R1 = 20\text{k}$, $R2 = 146\Omega$, $C1 = 30\text{pF}$.