

BCD DECADE COUNTER/STORAGE ELEMENT 4-BIT BINARY COUNTER/STORAGE ELEMENT

8280 8281

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

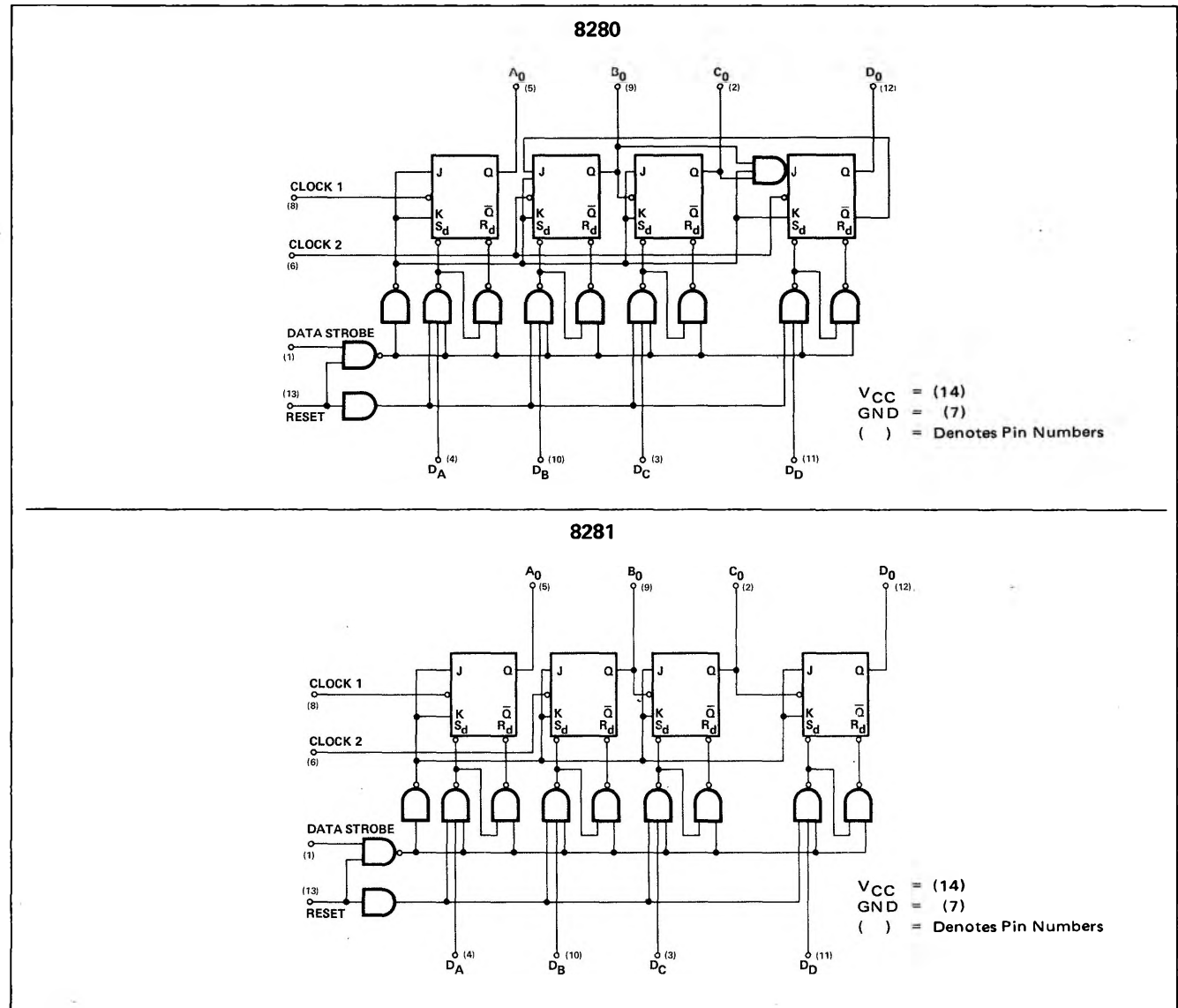
The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage (All Outputs)	2.6	3.5		V	0.8V	2.0V	2.0V				7
"0" Output Voltage (All Outputs)			0.4	V	0.8V	0.8V	0.8V				8
"0" Input Current											
Strobe	-0.1		-1.6	mA	0.4V						
Data Inputs	-0.1		-1.2	mA		0.4V					
Reset	-0.1		-3.2	mA			0.4V				
Clock 1	-0.1		-3.2	mA				0.4V			
Clock 2 (8280)	-0.1		-3.2	mA					0.4V		
Clock 2 (8281)	-0.1		-1.6	mA					0.4V		
"1" Input Current											
Strobe			40	μA	4.5V						
Data Inputs			40	μA		4.5V					
Reset			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2 (8280)			80	μA					4.5V		
Clock 2 (8281)			40	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		12
Input Voltage Rating all Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		10
Output Short Circuit Current	-10		-60	mA	0V					0V	

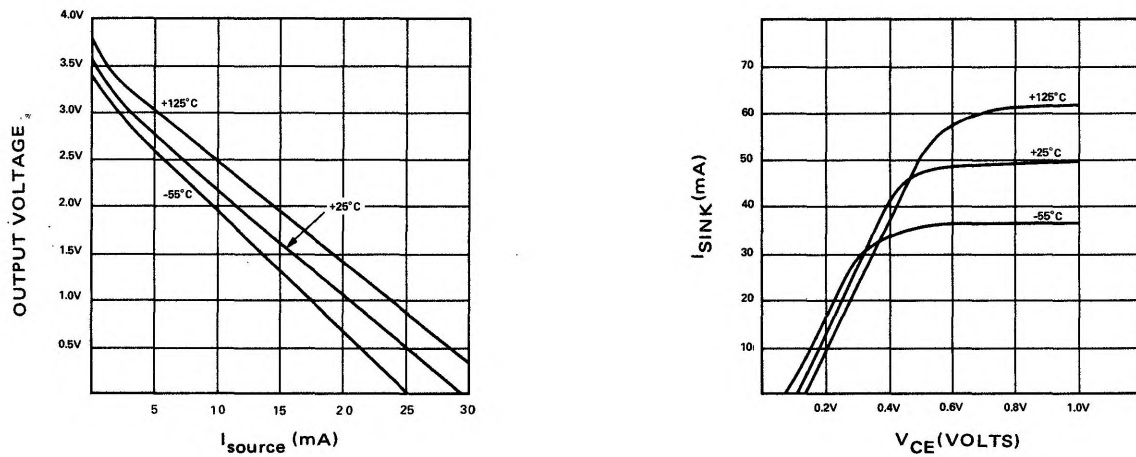
 $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode T_{on} Delay											
Bit A, B, C, D		15	25	ns							11
Clock Mode T_{off} Delay											
Bit A, B, C, D		15	25	ns							11
Data/Strobe t_{on} Delay											
Bit A, B, C, D		25	35	ns							11
Data/Strobe t_{off} Delay											
Bit A, B, C, D		30	40	ns							11
Toggle Rate	20	25		MHz							11
Strobe Pulse Width		20	35	ns					A _{OUT}		11
Reset Pulse Width		20	35	ns					A _{OUT}		11
Strobe Release Time		30	40	ns					A _{OUT}		11
Reset Release Time		50	75	ns					A _{OUT}		11

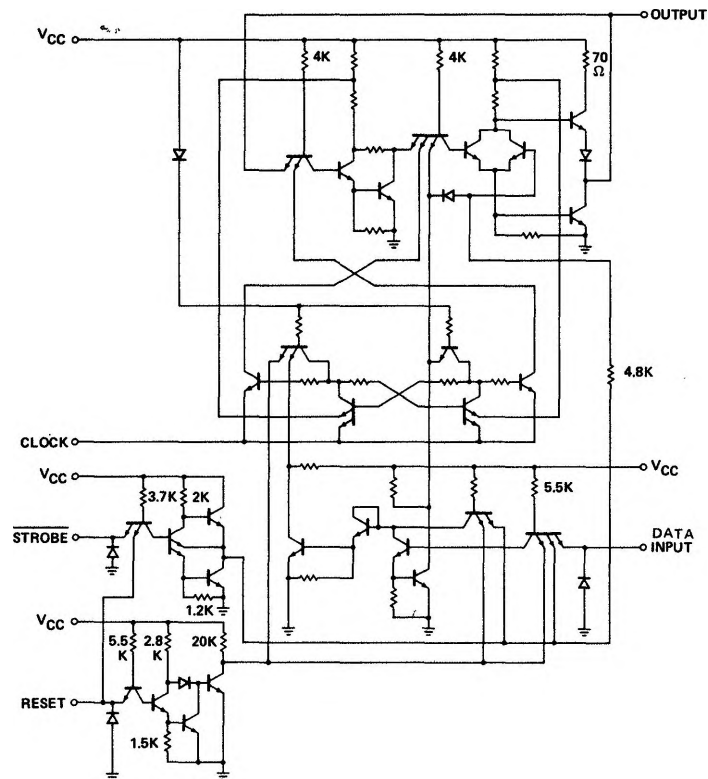
NOTES:

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND logic definition:
"UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each output and the associated data input independently.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- Manufacturer reserves the right to make design and process changes and improvements.
- Each input is tested separately.
- Refer to AC Test Figures.
- $V_{CC} = 5.25\text{V}$.

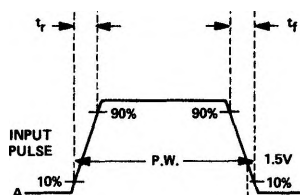
TYPICAL OUTPUT CHARACTERISTICS



SCHEMATIC DIAGRAM

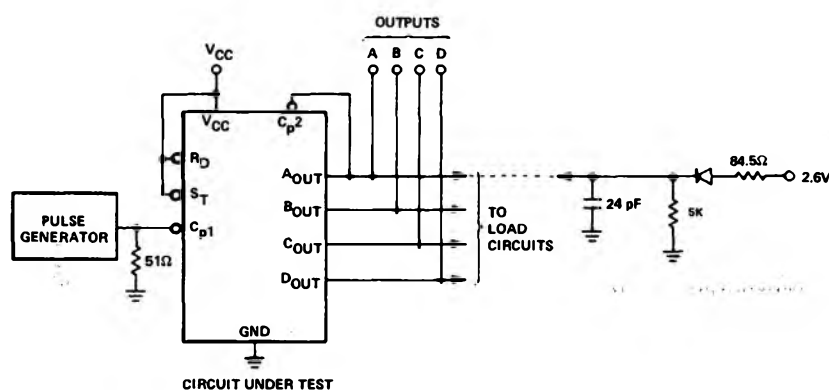


AC TEST FIGURES AND WAVEFORMS



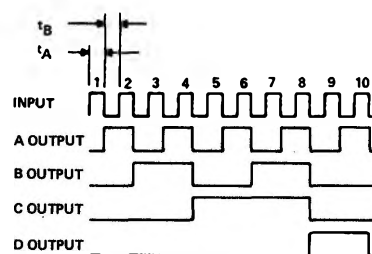
NOTE: Input pulse notations apply unless otherwise specified.

TOGGLE RATE

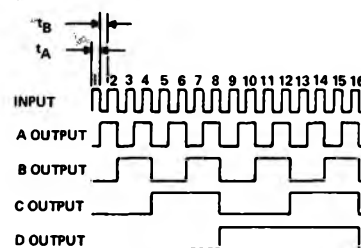
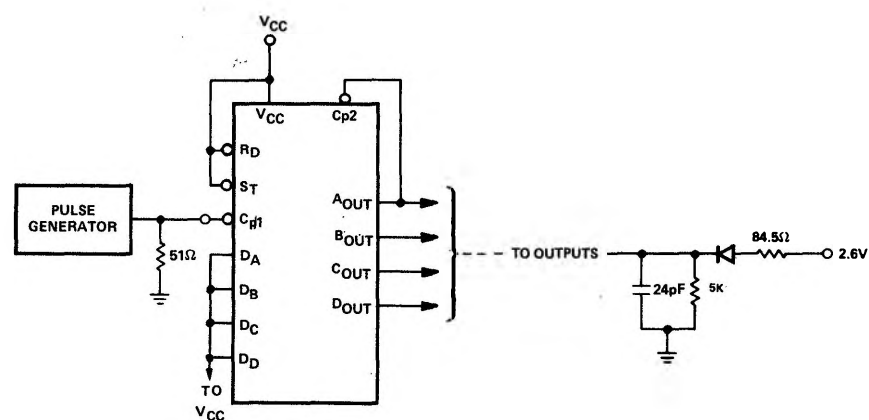


INPUT PULSE:
Amplitude = 2.6V
 $t_A = 25\text{ns}$, $t_B = 25\text{ns}$,
 $t_r = t_f = 5\text{ns max.}$

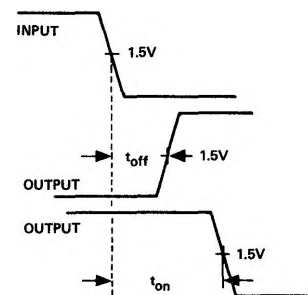
8280



8281

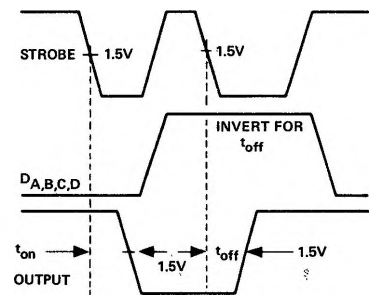
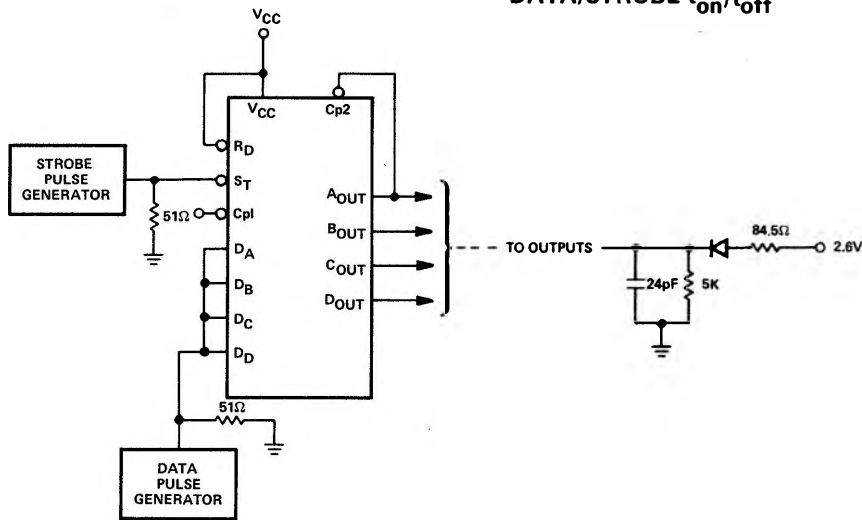
CLOCK MODE t_{on}/t_{off} DELAY

1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:



INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
 $t_r = t_f = 5\text{ns.}$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

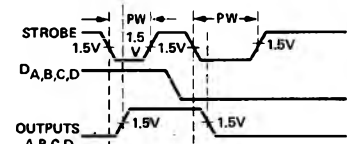
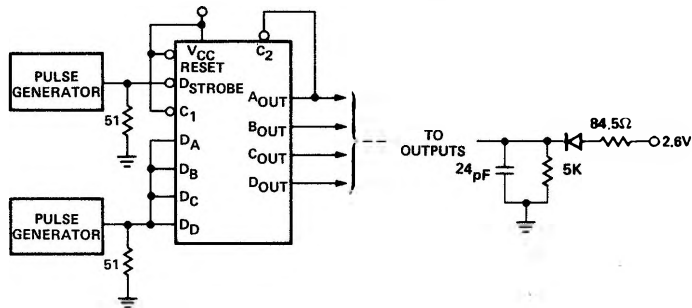
DATA/STROBE t_{on}/t_{off} 

Strobe, P.A. = 2.6V
 P.W. = 300ns, 50% to 50%
 PRR = 1 MHz
 $t_r = t_f = 5ns$
 Data, P.A. = 2.6V
 P.W. = 500ns
 PRR = 500 KHz
 $t_r = t_f = 5ns$

NOTES:

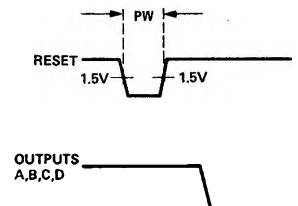
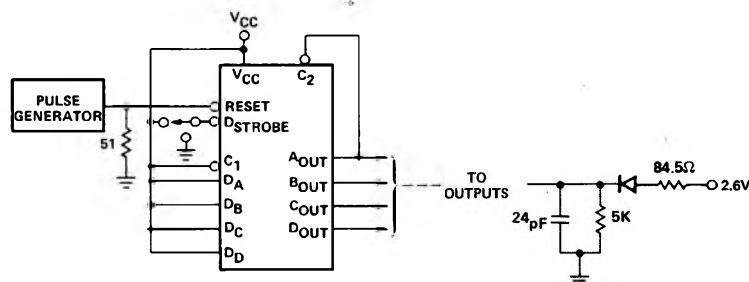
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{ MHz}$, $V_{ac} = 25\text{ mV}_{rms}$.
3. All diodes are 1N916.

MINIMUM STROBE PULSE WIDTH



INPUT PULSE:
 Amplitude = 2.6V
 $t_r = t_f = 5ns$

MINIMUM RESET PULSE WIDTH



INPUT PULSE:
 Amplitude = 2.6V
 $t_r = t_f = 5ns\text{ max.}$
 Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

