

DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.

The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus,

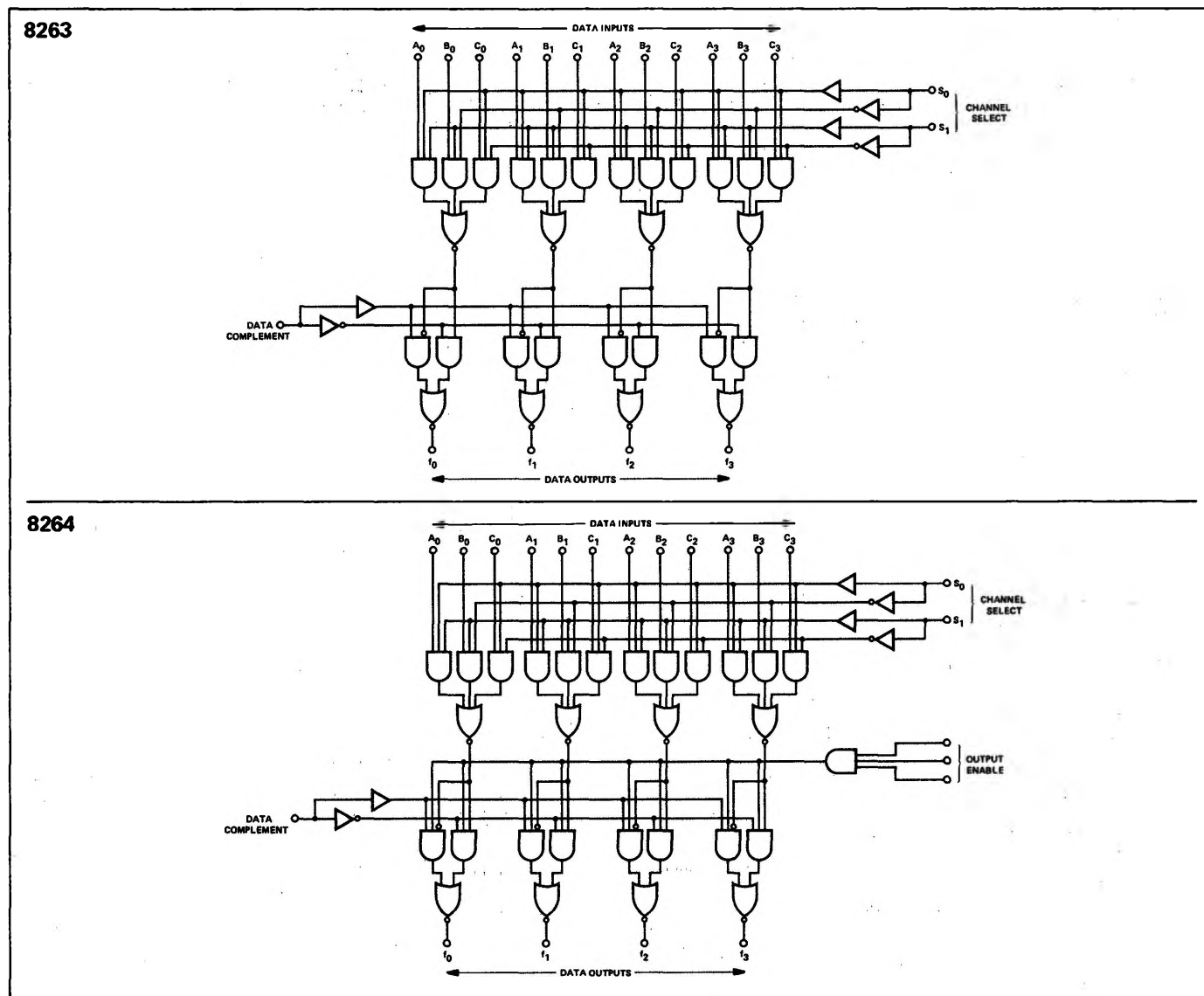
eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

TRUTH TABLE

Data Input	Channel Select	Data Complement	Output Enable (8264)	Data Outputs
$A_n B_n C_n$	$S_0 S_1$			
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	\bar{A}_n
x B_n x	0 1	1	1	\bar{B}_n
x x C_n	1 0	1	1	\bar{C}_n
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either State

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A _n	B _n	C _n	S ₀	S ₁	DATA COMP	OUTPUT ENABLE	OUTPUTS	
"1" Output Voltage (8263)	2.6	3.5		V	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V		800 μ A	8
"1" Output Leakage Current (8264)			200	μ A	2.0V	2.0V	2.0V	2.0V	2.0V	0.8V	2.0V		11
"0" Output Voltage (8263)			0.4	V	0.8V	0.8V	0.8V	2.0V	2.0V	0.8V		9.6mA	9
"0" Output Voltage (8264)			0.4	V	0.8V							16.0mA	11
"0" Input Current													
A _n	-0.1		-1.6	mA	0.4V								
B _n	-0.1		-1.6	mA		0.4V		0.4V					
C _n	-0.1		-1.6	mA			0.4V		0.4V				
OE, DC	-0.1		-1.6	mA						0.4V	0.4V		6
S ₀ , S ₁	-0.1		-3.2	mA				0.4V	0.4V				
"1" Input Current													
A _n			40	μ A	4.5V			0V	0V				
B _n			40	μ A		4.5V		0V	0V				
C _n			40	μ A			4.5V	0V					
OE, DC			40	μ A						4.5V	4.5V		
S ₀ , S ₁			40	μ A				4.5V	4.5V				

T_A = 25°C and V_{CC} = 5.0V

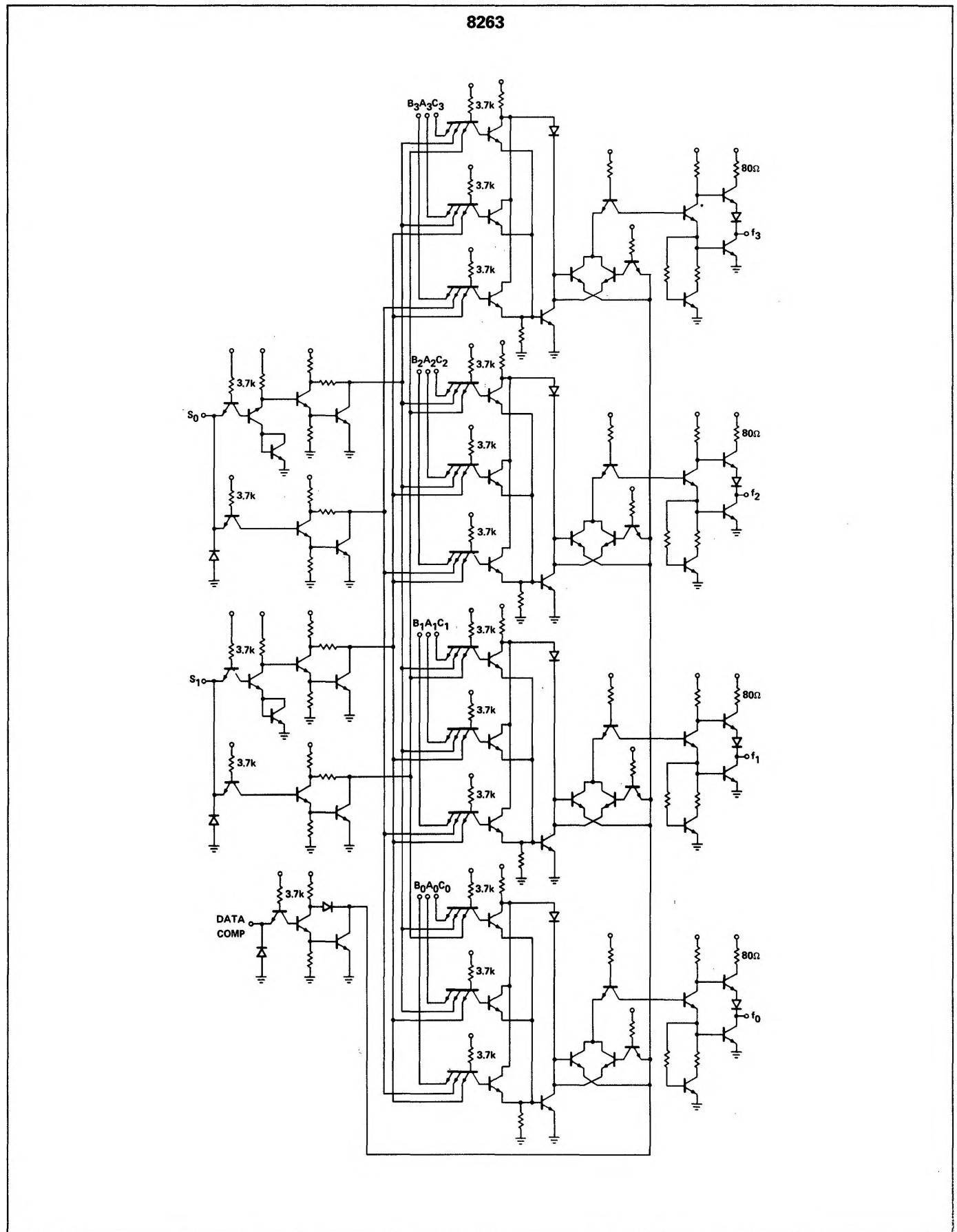
CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	A _n	B _n	C _n	S ₀	S ₁	DATA COMP	OUTPUT ENABLE	OUTPUTS	
Propagation Delay (8263)													
A _n to f _n		17	26	ns									10
S ₀ , S ₁ to f _n		25	36	ns									10
DC to f _n		17	26	ns									10
Propagation Delay (8264)													
A _n to f _n		25	36	ns									10
S ₀ , S ₁ to f _n		25	36	ns									10
DC to f _n		20	30	ns									10
OE to f _n		20	30	ns									10
Input Latch Voltage													
Rating													
A _n	5.5			V	10mA			0V	0V				12
B _n	5.5			V		10mA			0V				12
C _n	5.5			V			10mA	0V					12
S ₀	5.5			V				10mA					12
S ₁	5.5			V					10mA				12
DC	5.5			V						10mA			12
OE	5.5			V							10mA		12
Output Short Circuit Current	-20		-70									0V	
Power/Current Consumption													14
(8263)		378/	420/	mW/				0V					
		72	80	mA									
(8264)		400/	475/	mW/				0V					
		76	90.4	mA									

NOTES:

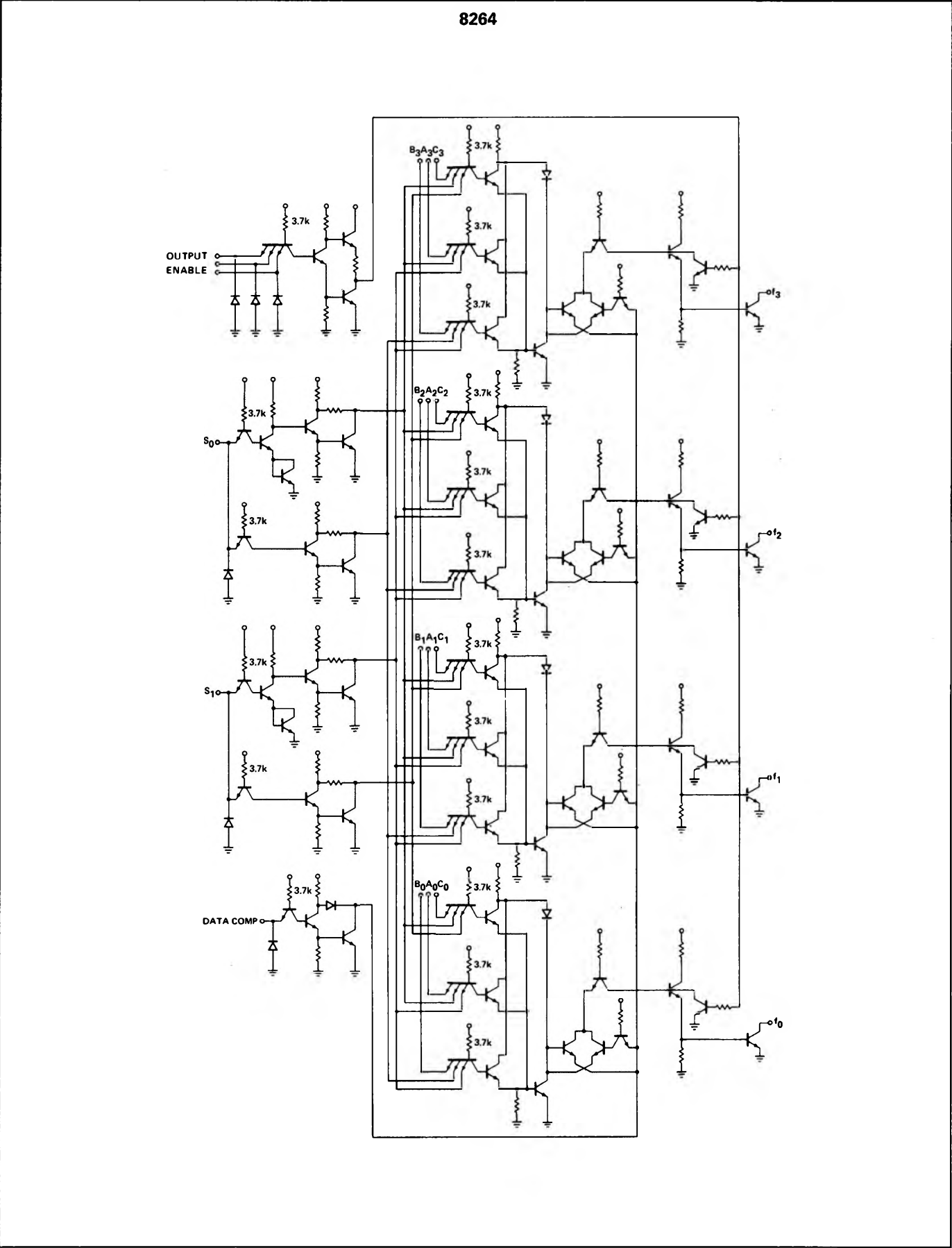
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND Logic Definition:
"UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Capacitance as measured on Boonton Electric Corporation

- Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25m Vrms. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC}.
- Refer to AC Test Figure.
- Connect an external 1k \pm 1% resistor from V_{CC} to the output for this test.
- This test guarantees operation free of input latch-up over the specified operating supply voltage range.
- Manufacturer reserves the right to make design and process changes and improvements.
- V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAMS



SCHEMATIC DIAGRAMS (Cont'd)



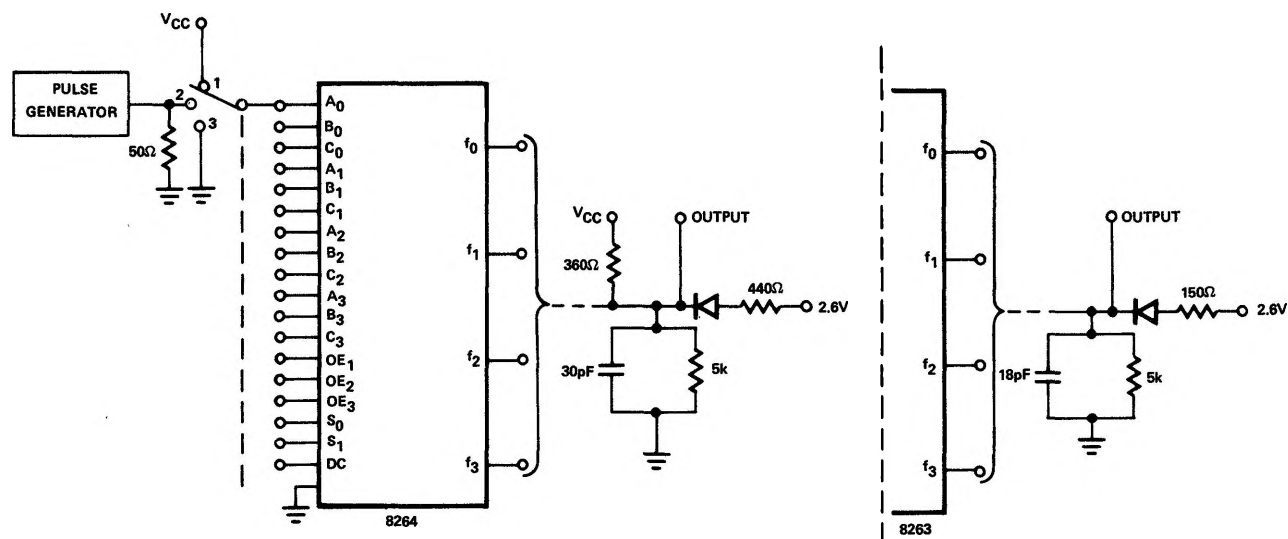
AC TESTING

Step No.	Delay From-To	Switching Positions																			Waveform Types
		Driven Inputs	Other Inputs																		
			A ₀	B ₀	C ₀	A ₁	B ₁	C ₁	A ₂	B ₂	C ₂	A ₃	B ₃	C ₃	OE	OE	OE	S ₀	S ₁	DC	
1	A _n to f _n	2	2	1	1	2	1	1	2	1	1	2	1	1	1	1	1	1	1	1	C, D
2	S ₀ to f _n	2	3	1	1	3	1	1	3	1	1	3	1	1	1	1	1	2	1	1	A, B
3	S ₀ to f _n	2	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	1	C, D
4	S ₁ to f _n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	C, D
5	DC to f _n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	C, D
6	OE _n to f _n	2	1	1	1	1	1	1	1	1	1	1	1	1	*	*	*	1	1	1	C, D

NOTE: Step number 6 is for 8264 only.

* Test one input at a time - others remain at "1".

AC TEST FIGURE AND WAVEFORMS



NOTE:

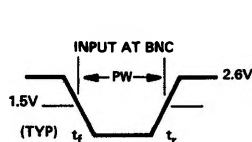
1. Scope terminals to be $< 1\frac{1}{2}$ " from package pins.
2. Position 1 on switch provides a logical "1".

Position 2 on switch provides pulse.

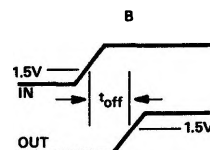
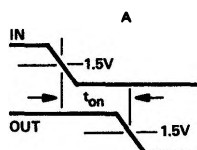
Position 3 on switch provides a logical "0".

3. All measurements are made at 1.5V level.
4. See truth table for logical conditions.

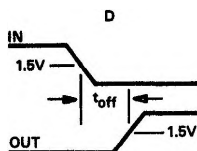
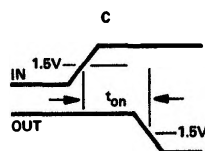
NON-INVERTING PATHS



$t_r = t_f \leq 3ns$
 Amplitude = 2.6V
 PW = 200ns
 PRR = 1MHz



INVERTING PATHS



TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to select a particular 8264. All non-selected 8264's have their outputs in the logic "1" condition, thus allowing the selected multiplexer to predominate.

Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3-register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263. Now there are three different pre-settable 4-bit words that can be chosen by the 8264. By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

EXPANDING THE 8264

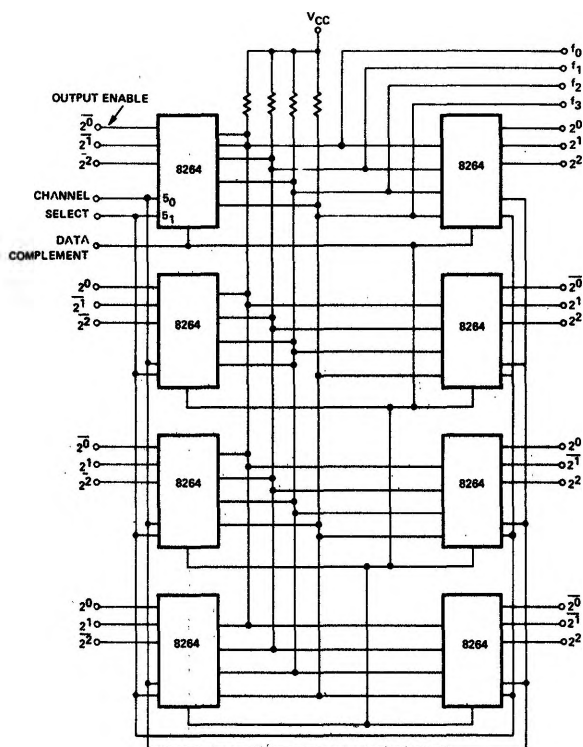


FIGURE 1

VARIABLE MODULUS COUNTER

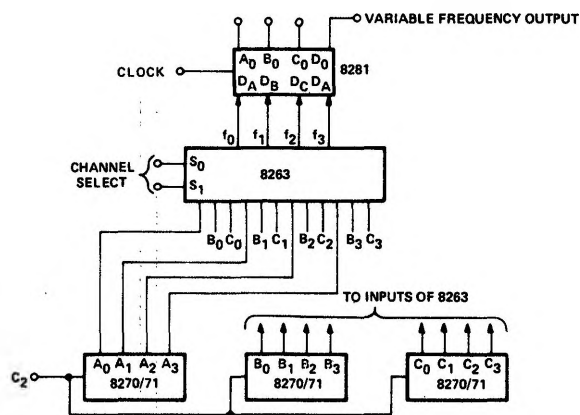


FIGURE 2