



8228/8238

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- Single Chip System Control for MCS-80™ Systems
- Built-in Bi-Directional Bus Driver for Data Bus Isolation
- Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge
- User Selected Single Level Interrupt Vector (RST 7)
- 28 Pin Dual In-Line Package
- Reduces System Package Count
- *8238 Has Advanced IOW/MEMW for Large System Timing Control

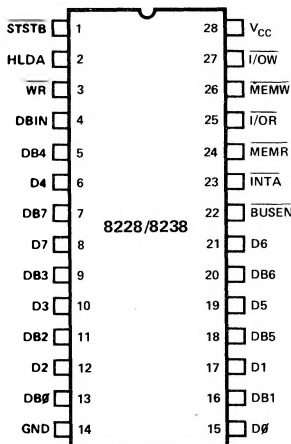
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

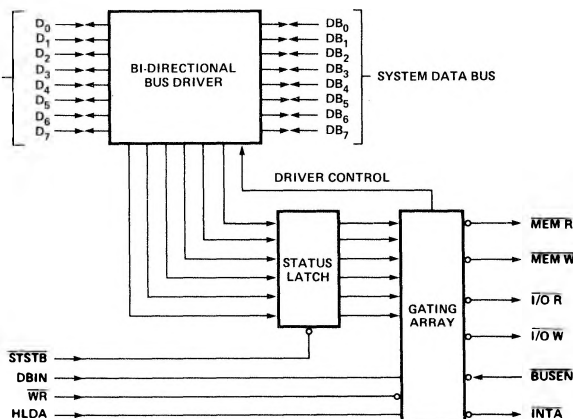
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228/8238 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

FUNCTIONAL DESCRIPTION

General

The 8228 and 8238 are single chip System Controllers and Data Busdrivers for the 8080 Microcomputer System. They generate all control signals required to directly interface MCS-80™ family RAM, ROM, and I/O components.

Schottky Bipolar technology is used to maintain low delay times and provide high output drive capability to support small to medium systems.

Bi-Directional Bus Driver

An eight bit, bi-directional bus driver is provided to buffer the 8080 data bus from Memory and I/O devices. The 8080A data bus has an input requirement of 3.3 volts (min) and can drive (sink) a maximum current of 1.9mA. The 8228/38 data bus driver assures that these input requirements will be not only met but exceeded for enhanced noise immunity. Also, on the system side of the driver adequate drive current is available (10mA Typ.) so that a large number of Memory and I/O devices can be directly connected to the bus.

The Bi-Directional Bus Driver is controlled by signals from the Gating Array so that proper bus flow is maintained and its outputs can be forced into their high impedance state (3-state) for DMA activities.

Status Latch

At the beginning of each machine cycle the 8080 CPU issues "status" information on its data bus that indicates the type of activity that will occur during the cycle. The 8228/38 stores this information in the Status Latch when the $\overline{STSTB}$ input goes "low". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array

The Gating Array generates control signals ($\overline{MEM R}$, $\overline{MEM W}$,

$\overline{I/O R}$, $\overline{I/O W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch with signals from the 8080 CPU ($\overline{DBIN}$, $\overline{WR}$, and $\overline{HLDA}$).

The "read" control signals ($\overline{MEM R}$, $\overline{I/O R}$ and $\overline{INTA}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the $\overline{DBIN}$ input from the 8080 CPU.

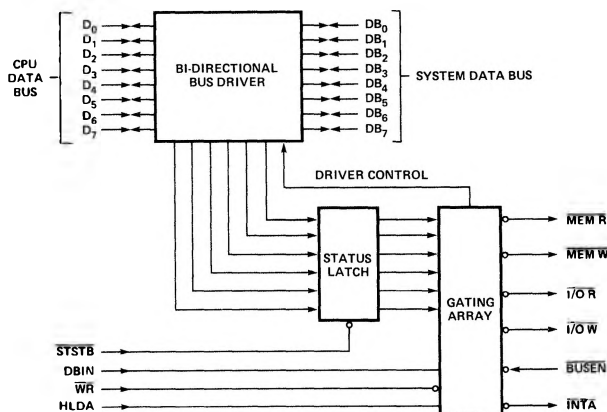
The "write" control signals from the 8228 ($\overline{MEM W}$, $\overline{I/O W}$) are derived from the logical combination of the appropriate Status Bit (or bits) and the $\overline{WR}$ input from the 8080 CPU. The write signals coming from the 8238 are advanced for large system timing control.

All Control Signals are "active low" and directly interface to MCS-80 family RAM, ROM and I/O components.

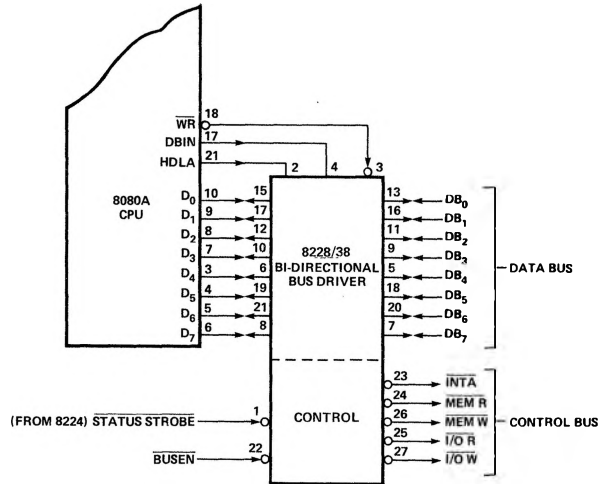
The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the 8228/38. If only one basic vector is needed in the interrupt structure, such as in small systems, the 8228/38 can automatically insert a RST 7 instruction onto the bus at the proper time. To use this option, simply connect the $\overline{INTA}$ output of the 8228/38 (pin 23) to the +12 volt supply through a series resistor (1K ohms). The voltage is sensed internally by the 8228/38 and logic is "set-up" so that when the $\overline{DBIN}$ input is active a RST 7 instruction is gated on to the bus when an interrupt is acknowledged. This feature provides a single interrupt vector with no additional components, such as an interrupt instruction port.

When using **CALL** as an Interrupt instruction the 8228/38 will generate an $\overline{INTA}$ pulse for each of the three bytes.

The $\overline{BUSEN}$ (Bus Enable) input to the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "one". If $\overline{BUSEN}$ is a "zero" normal operation of the data buffer and control signals take place.



8228/38 BLOCK DIAGRAM



STATUS WORD CHART

		TYPE OF MACHINE CYCLE										N STATUS WORD
	DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE	HALT ACKNOWLEDGE	INTERRUPT ACKNOWLEDGE WHILE HALT
D0	INTA	0	0	0	0	0	0	0	1	0	1	
D1	WO	1	1	0	1	0	1	0	1	1	1	
D2	STACK	0	0	0	1	1	0	0	0	0	0	
D3	HLTA	0	0	0	0	0	0	0	0	1	1	
D4	OUT	0	0	0	0	0	0	1	0	0	0	
D5	M1	1	0	0	0	0	0	0	1	0	1	
D6	INP	0	0	0	0	0	1	0	0	0	0	
D7	MEMR	1	1	0	1	0	0	0	0	1	0	

CONTROL SIGNALS

INTA (NONE)

INTA

I/O W

I/O R

MEM W

MEM R

MEM W

MEM R

MEM R

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-0°C to 70°C
Storage Temperature	-65°C to 150°C
Supply Voltage, V_{CC}	-0.5V to +7V
Input Voltage	-1.5V to +7V
Output Current	100mA

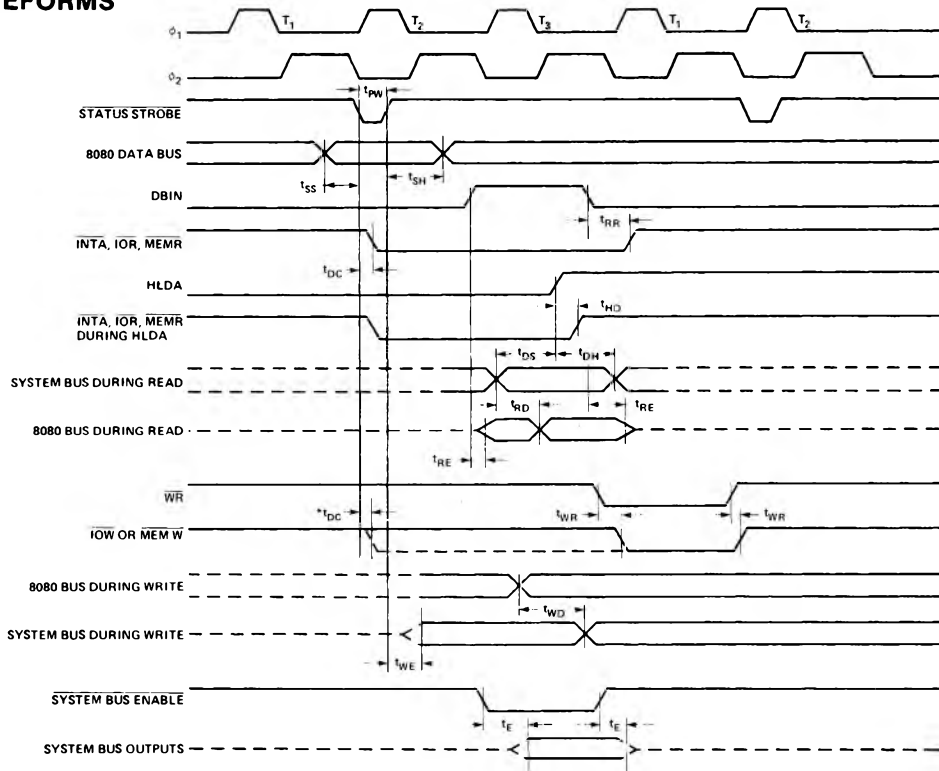
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = 5\text{V} \pm 5\%$.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. [1]	Max.		
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	$V_{CC}=4.75\text{V}; I_C=-5\text{mA}$
I_F	Input Load Current, STSTB			500	μA	$V_{CC}=5.25\text{V}$ $V_F=0.45\text{V}$
	D_2 & D_6			750	μA	
	$D_0, D_1, D_4, D_5,$ & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current STSTB			100	μA	$V_{CC}=5.25\text{V}$ $V_R=5.25\text{V}$
	DB_0 - DB_7			20	μA	
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	$V_{CC}=5\text{V}$
I_{CC}	Power Supply Current		140	190	mA	$V_{CC}=5.25\text{V}$
V_{OL}	Output Low Voltage, D_0 - D_7			.45	V	$V_{CC}=4.75\text{V}; I_{OL}=2\text{mA}$
	All Other Outputs			.45	V	$I_{OL}=10\text{mA}$
V_{OH}	Output High Voltage, D_0 - D_7	3.6	3.8		V	$V_{CC}=4.75\text{V}; I_{OH}=-10\mu\text{A}$
	All Other Outputs	2.4			V	$I_{OH}=-1\text{mA}$
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	$V_{CC}=5\text{V}$
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	$V_{CC}=5.25\text{V}; V_O=5.25$
				-100	μA	$V_O=.45\text{V}$
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED IOW/MEMW FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 5\text{V} \pm 5\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	$C_L = 100\text{pF}$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100\text{pF}$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25\text{pF}$
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25\text{pF}$
t_{WR}	Delay from WR to Control Outputs	5	45	ns	$C_L = 100\text{pF}$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100\text{pF}$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100\text{pF}$
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7		30	ns	$C_L = 100\text{pF}$
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	$C_L = 100\text{pF}$

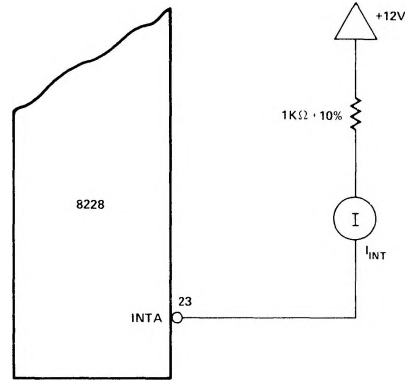
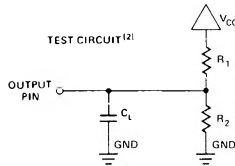
CAPACITANCE

This parameter is periodically sampled and not 100% tested.

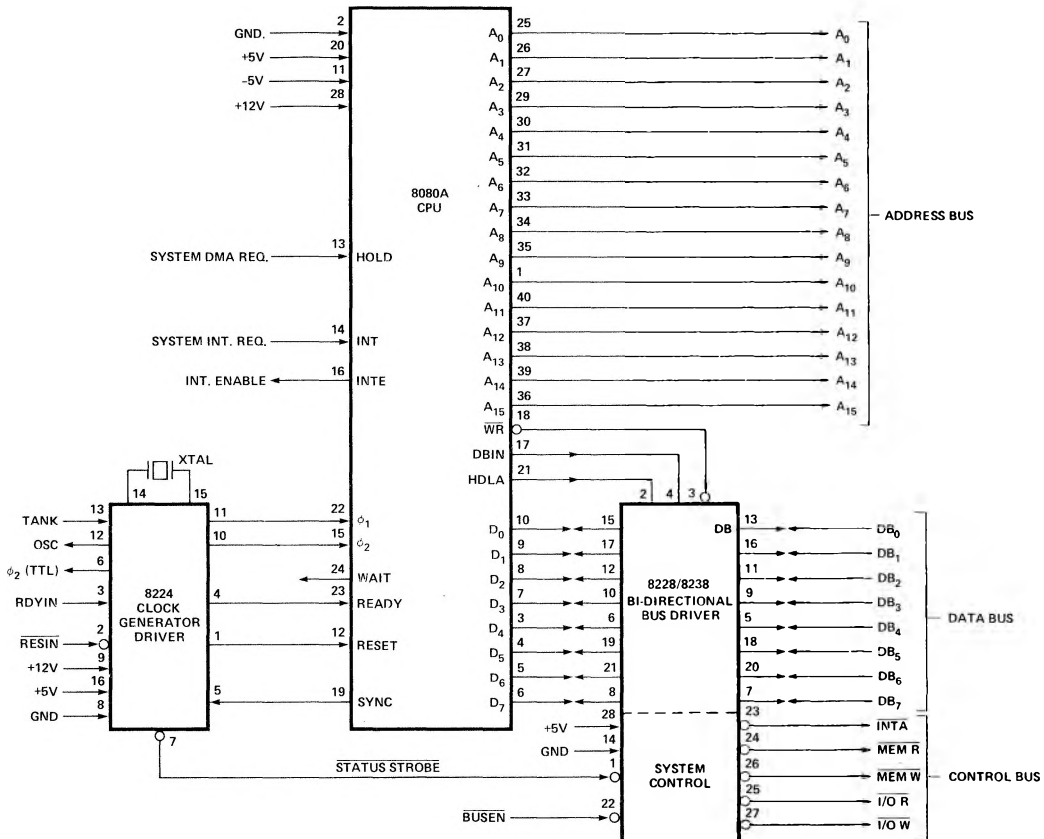
Symbol	Parameter	Limits			Unit
		Min.	Typ. ^[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1MHz$.

Note 2: For D_0 - D_7 : $R_1 = 4K\Omega$, $R_2 = \infty\Omega$,
 $C_L = 25pF$. For all other outputs:
 $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



INTA Test Circuit (for RST 7)



CPU Standard Interface