signetics

256 BIT ROM, ASCII TO EBCDIC CODE CONVERTER, ALPHABET ONLY

8224

REFER TO PAGE 13 FOR B, E AND R PACKAGE PIN CONFIGURATIONS.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8224 is a TTL 256 Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Select input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

This device has been programmed to convert the seven bit ASC II alphabet code to the 8 bit EBCDIC Alphabet code. The conversion includes the letters A through Z. With the addition of gating circuitry, the 8224 will convert both upper case and lower case letters.

Customer specified patterns are also available as custom products. Refer to page 199 for Truth Table/Order Blank.

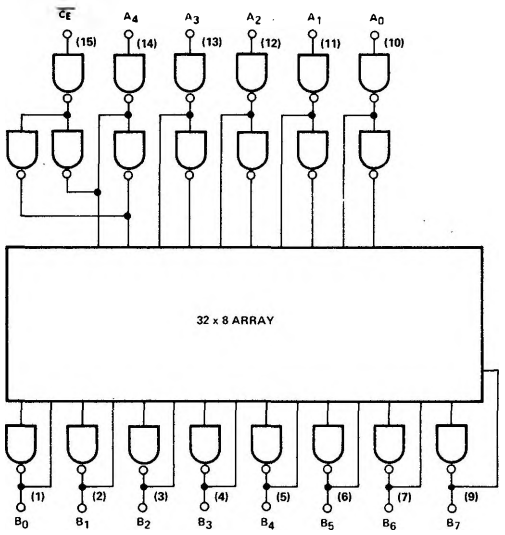
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- CHIP ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATOR
CONTROL STORE

LOGIC DIAGRAM



V_{CC}-16, GND-8
(x) DENOTES PIN NUMBER

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
"1" Output Leakage Current		100	μA	5.00			2.0V		13
"0" Output Voltage		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	5.00	0.8V	2.0V	0.8V	9.6mA	6,10
		0.4	V	4.75	0.8V	2.0V	0.8V	9.6mA	6,10
"1" Input Current									
An, Address		40	μA	5.25		4.5V	4.5V		
$\overline{\text{Chip Enable}}$ Input		80	μA						
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1	-1.6	mA	5.25	0.4V		0.4V		

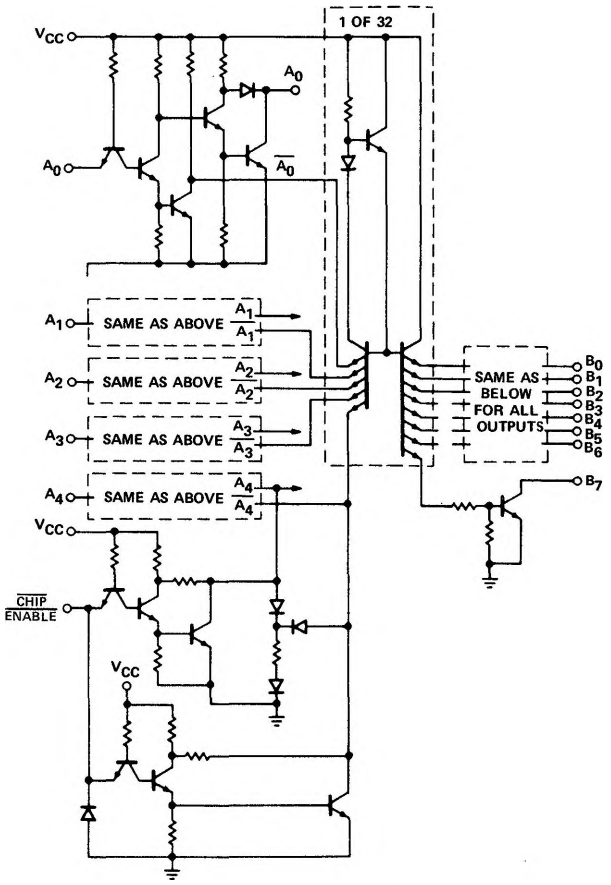
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS			TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	MAX.	UNITS	V_{CC}	A_n "0"	A_n "1"	$\overline{\text{CHIP ENABLE}}$		
Propagation Delay									
An to Bn		50	ns	5.00				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to Bn		50	ns	5.00		4.5V	4.5V	DC F.O.=12	7,12
Power Consumption		400	mW	5.25		4.5V	4.5V		
Input Latch Voltage	5.5		V	5.00	10mA		10mA		11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.

SCHEMATIC DIAGRAM



CODE CONVERSION ASCII TO EBCDIC (UPPER & LOWER CASE LETTERS ONLY)

ASC II CODE							CHARACTER	EBCDIC CODE
b_7	b_6	b_5	b_4	b_3	b_2	b_1		0 1 2 3 4 5 6 7
0	0	0	X	X	X	X	--	Not Decoded
0	0	1	X	X	X	X	--	Not Decoded
0	1	0	X	X	X	X	--	Not Decoded
0	1	1	X	X	X	X	--	Not Decoded
1	0	0	0	0	0	0	--	Not Decoded
1	0	0	0	0	0	1	A	1 1 0 0 0 0 0 1
1	0	0	0	0	1	0	B	1 1 0 0 0 0 1 0
1	0	0	0	0	1	1	C	1 1 0 0 0 0 1 1
1	0	0	0	1	0	0	D	1 1 0 0 0 1 0 0
1	0	0	0	1	0	1	E	1 1 0 0 0 1 0 1
1	0	0	0	1	1	0	F	1 1 0 0 0 1 1 0
1	0	0	0	1	1	1	G	1 1 0 0 0 1 1 1
1	0	0	1	0	0	0	H	1 1 0 0 1 0 0 0
1	0	0	1	0	0	1	I	1 1 0 0 1 0 0 1
1	0	0	1	0	1	0	J	1 1 0 1 0 0 0 1
1	0	0	1	0	1	1	K	1 1 0 1 0 0 1 0
1	0	0	1	1	0	0	L	1 1 0 1 0 0 1 1
1	0	0	1	1	0	1	M	1 1 0 1 0 1 0 0
1	0	0	1	1	1	0	N	1 1 0 1 0 1 0 1
1	0	0	1	1	1	1	O	1 1 0 1 0 1 1 0
1	0	1	0	0	0	0	P	1 1 0 1 0 1 1 1
1	0	1	0	0	0	1	Q	1 1 0 1 1 0 0 0
1	0	1	0	0	1	0	R	1 1 0 1 1 0 0 1
1	0	1	0	0	1	1	S	1 1 1 0 0 0 1 0
1	0	1	0	1	0	0	T	1 1 1 0 0 0 1 1
1	0	1	0	1	0	1	U	1 1 1 0 0 1 0 0
1	0	1	0	1	1	0	V	1 1 1 0 0 1 0 1
1	0	1	0	1	1	1	W	1 1 1 0 0 1 1 0
1	0	1	1	0	0	0	X	1 1 1 0 0 1 1 1
1	0	1	1	0	0	1	Y	1 1 1 0 1 0 0 0
1	0	1	1	0	1	0	Z	1 1 1 0 1 0 0 1
1	0	1	1	0	1	1	--	1 Not Decoded
1	0	1	1	1	0	0	--	1 Not Decoded
1	0	1	1	1	0	1	--	1 Not Decoded
1	0	1	1	1	1	0	--	1 Not Decoded
1	0	1	1	1	1	1	--	1 Not Decoded
1	1	0	0	0	0	0	--	1 Not Decoded
1	1	0	0	0	0	1	a	1 0 0 0 0 0 0 1
1	1	0	0	0	1	0	b	1 0 0 0 0 0 1 0
1	1	0	0	0	1	1	c	1 0 0 0 0 0 1 1
1	1	0	0	1	0	0	d	1 0 0 0 0 1 0 0
1	1	0	0	1	0	1	e	1 0 0 0 0 1 0 1
1	1	0	0	1	1	0	f	1 0 0 0 0 1 1 0
1	1	0	0	1	1	1	g	1 0 0 0 0 1 1 1
1	1	0	1	0	0	0	h	1 0 0 0 1 0 0 0
1	1	0	1	0	0	1	i	1 0 0 0 1 0 0 1
1	1	0	1	0	1	0	j	1 0 0 1 0 0 0 1
1	1	0	1	0	1	1	k	1 0 0 1 0 0 1 0
1	1	0	1	1	0	0	l	1 0 0 1 0 0 1 1
1	1	0	1	1	0	1	m	1 0 0 1 0 1 0 0
1	1	0	1	1	1	0	n	1 0 0 1 0 1 0 1
1	1	0	1	1	1	1	o	1 0 0 1 0 1 1 0
1	1	1	0	0	0	0	p	1 0 0 1 0 1 1 1
1	1	1	0	0	0	1	q	1 0 0 1 1 0 0 0
1	1	1	0	0	1	0	r	1 0 0 1 1 0 0 1
1	1	1	0	0	1	1	s	1 0 1 0 0 0 1 0
1	1	1	0	1	0	0	t	1 0 1 0 0 0 1 1
1	1	1	0	1	0	1	u	1 0 1 0 0 1 0 0
1	1	1	0	1	1	0	v	1 0 1 0 0 1 0 1
1	1	1	0	1	1	1	w	1 0 1 0 0 1 1 0
1	1	1	1	0	0	0	x	1 0 1 0 0 1 1 1
1	1	1	1	0	0	1	y	1 0 1 0 1 0 0 0
1	1	1	1	0	1	0	z	1 0 1 0 1 0 0 1
1	1	1	1	0	1	1	--	Not Decoded
1	1	1	1	1	0	0	--	Not Decoded
1	1	1	1	1	0	1	--	Not Decoded
1	1	1	1	1	1	0	--	Not Decoded
1	1	1	1	1	1	1	--	Not Decoded

TRUTH TABLES

INPUT PINS						OUTPUT PINS							
15	14	13	12	11	10	9	7	6	5	4	3	2	1
$\overline{CE}$	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	0	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1	0	0	0	1	1
0	0	0	1	1	1	1	1	1	0	0	0	1	1
0	0	1	0	0	0	0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1	0	0	1	1
0	0	1	0	1	0	1	0	0	0	1	0	1	1
0	0	1	0	1	1	0	1	0	0	1	0	1	1
0	0	1	1	0	0	1	1	0	0	1	0	1	1
0	0	1	1	0	1	0	0	1	0	1	0	1	1
0	0	1	1	1	0	1	0	1	0	1	0	1	1
0	1	0	0	0	0	1	1	1	0	1	0	1	1
0	1	0	0	0	1	0	0	0	1	1	0	1	1
0	1	0	0	1	0	1	0	0	1	1	0	1	1
0	1	0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	1	0	0	1	1	0	0	0	1	1	1
0	1	0	1	0	1	0	0	1	0	0	1	1	1
0	1	0	1	1	0	1	0	1	0	0	1	1	1
0	1	0	1	1	1	0	1	1	0	0	1	1	1
0	1	1	0	0	0	1	1	1	0	0	1	1	1
0	1	1	0	0	1	0	0	0	1	0	1	1	1
0	1	1	0	1	0	1	0	0	1	0	1	1	1
0	1	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	x	x	x	x	x	1	1	1	1	1	1	1	1

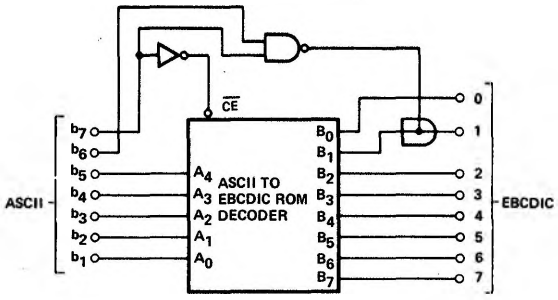
TYPICAL APPLICATIONS

To select the ROM only when addressed by an upper or lower case alphabet character, the following truth table applies:

	Upper Case		Lower Case	
ASCII	0	0	1	1
ASCII	0	1	0	1
$\overline{\text{CHIP ENABLE}} = \overline{B_7}$	1	1	0	0
EBCDIC #1 OUTPUT = $\overline{B_6 \cdot B_7}$	1	1	1	0

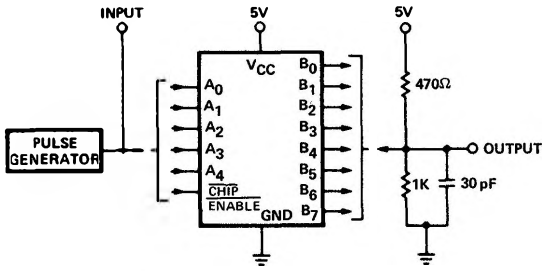
Thus, the ASCII to EBCDIC ROM standard product plus gating as shown performs the complete conversion.

TYPICAL APPLICATIONS (Cont'd)



GROUND PIN 15 WHEN TESTING ADDRESS-OUTPUT DELAYS

AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
Amplitude = 3.0V
tr = tf = 5ns
PW = 200ns (50% DUTY CYCLE)