signetics

8-BIT CONTENT ADDRESSABLE MEMORY (4x2 CAM) 8220

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{nj}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

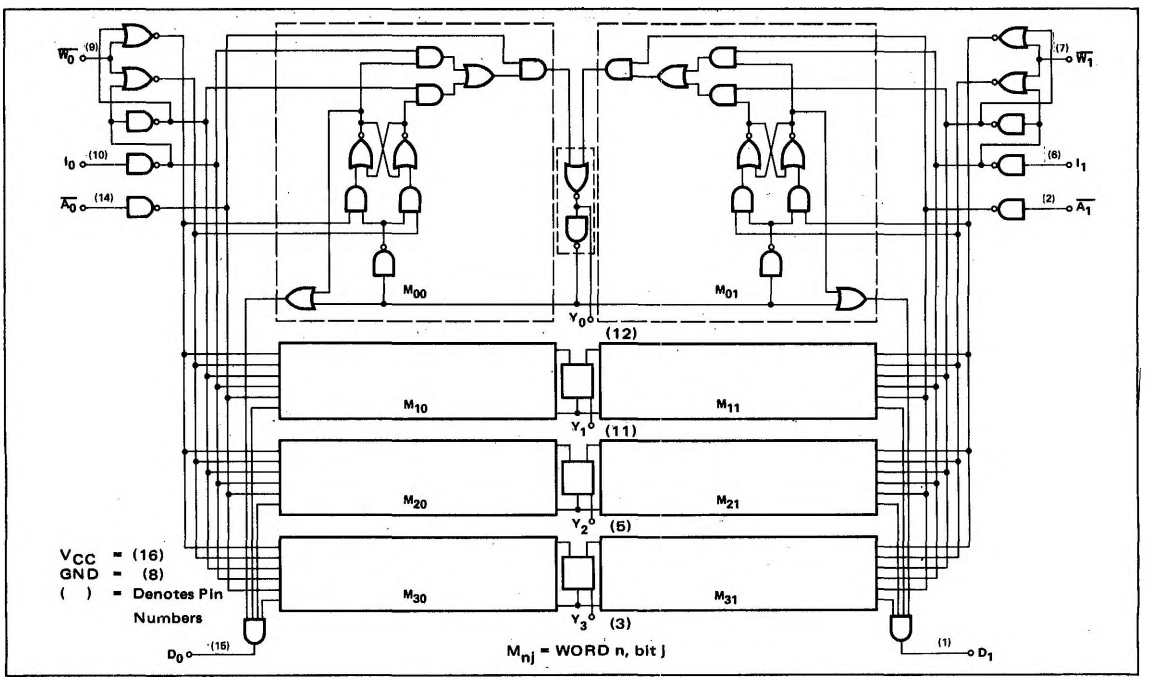
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

DATA-TO-MEMORY COMPARISON
PATTERN RECOGNITION
HIGH SPEED INFORMATION RETRIEVAL
CACHE MEMORY
AUTO CORRELATION
VIRTUAL MEMORY
LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS				$\overline{Wj}$	$\overline{Aj}$	I_j	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	μA		2.0V					10
Dj			100	μA				0V	0V		10
"1" Input Current											
Ij and $\overline{A_j}$			40	μA		4.5V	4.5V				
$\overline{W_j}$			80	μA	4.5V						
"0" Input Current											
Ij, Yn and $\overline{Aj}$	-0.1		-1.2	mA		0.4V	0.4V	0.4V			
$\overline{W_j}$			-2.4	mA							

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				Wj	Aj	Tj	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
Delay Time											
Associate ($\overline{Aj}$ to Yn)		20	30	ns							8, 11
Associate (Ij to Yn)		35	45	ns							8, 11
Read-Out (Yn to Dj)		30	40	ns							8, 11
Write-In to Read-Out ($\overline{Wj}$ to Dj)		45	60	ns							
Write Pulse Width		20	35	ns							
Power Consumption			590/ 118	mW/mA							

NOTES:

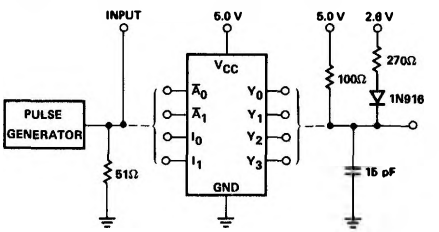
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Prior to this test write in a "0" in all or desired Memory cells as follows: Wj = Ij = 0V, Aj = V_{CC}.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Connect an external 1K ohm + 1% resistor from V_{CC} to the output terminal for this test.
11. See AC test Figures on the following pages.

MODE OF OPERATION

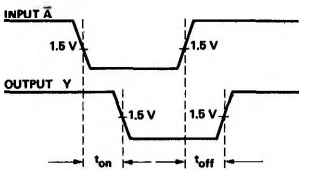
FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)	FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x	NO OPERATION	HOLD	1 1 1 1 x x	NO OPERATION
ASSOCIATE	1 1 1 0 x x	Question: ? $I_1=M_{i1}$ — Answer: YES — $Y_i=1, Y_k=0$; NO — $Y_i=Y_k=0$	WRITE-IN	1 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 into M_{i1}
				0 1 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_0 into M_{i0}
	1 1 0 1 x x	Question: ? $I_0=M_{i0}$ — Answer: YES — $Y_i=1, Y_k=0$; NO — $Y_i=Y_k=0$		0 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 and I_0 into M_{i1} and M_{i0}
	1 1 0 0 x x	Question: ? $I_1=M_{i1}$ and $I_0=M_{i0}$ — Answer: YES — $Y_i=1, Y_k=0$; NO — $Y_i=Y_k=0$	READ-OUT	1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_0 = 1 - IF M_{i0}=1, 0 - IF M_{i0}=0
				1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_1 = 1 - IF M_{i1}=1, 0 - IF M_{i1}=0
				1 1 1 1 x x	Forced Y_i=0, Y_k=0: $D_0=D_1=1$

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY

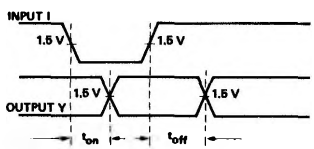


ASSOCIATE DELAY



NOTES:
1. When checking $\overline{A_0}$ let $\overline{A_1}$ = "1" and when checking $\overline{A_1}$ let $\overline{A_0}$ = "1".
2. $\overline{W_0}$ = $\overline{W_1}$. = "1".

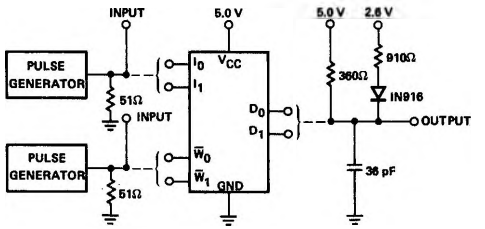
INPUT DELAY

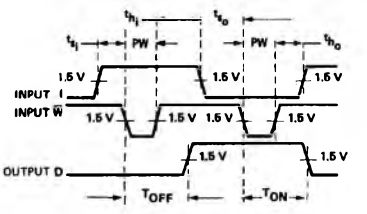


NOTES:
1. When checking I_1, $\overline{A_1}$ = "0" and $\overline{A_0}$ = "1" and when checking I_0, $\overline{A_0}$ = "0" and $\overline{A_1}$ = "1"
2. $\overline{W_0}$ = $\overline{W_1}$ = "1".

AC TEST FIGURES AND WAVEFORMS (Cont'd)

WRITE DELAY

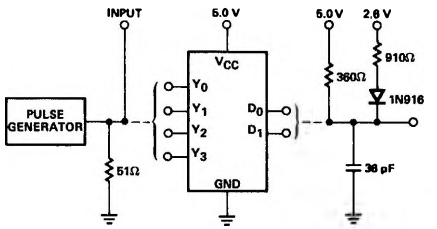


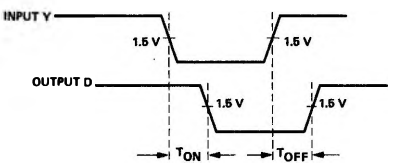


t_{si} = "1" set-up time.
t_{so} = "0" set-up time.
t_{hi} = "1" hold time.
t_{ho} = "0" hold time.
PW = Pulse width

NOTES:
1. $A_0 = \overline{A}_1$ = "1".
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY





NOTES:
1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1$ = "1".
3. $\overline{A}_0 = \overline{A}_1$ = "1".
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:
1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
   Frequency: 10 MHz ±5 MHz
   Amplitude: 0V to 3V
   Rise & Fall Times: 5 ns ±2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

I_j — Data Inputs
Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

$\overline{A}_j$ — Associate Controls
A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. Y_n = "1" = Match, Y_n = "0" Mismatch). A logical "1" at this pin forces all Y_n to a "1".

$\overline{W}_j$ — Write Enable
A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

Y_n — "Associate" Output and Address Selection Control
During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that A = 1 forces all Y_n = 1).

D_j — Data Output
These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under "Y_n" above.

GLOSSARY OF TERMS – SUBSCRIPTS

A.
- n = Word number = 0, 1, 2 and 3
- j = Bit number = 0 or 1
- i = Input/Output number(s) associated with cell(s) upon which a "Write-in", "Read-out" or other function is being performed.
- k = Input/Output number(s) other than "i" above.
- M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples
1. I_j for bit "1" equals I_1.
2. $M_{nj} = M_{10}$ = word "1" bit "0".
3. Y_i = 0, Y_k = 1: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3} = 0$ and $Y_{0,2} = 1$.

APPLICATION: LEARNING MEMORY

This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning" i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

By monitoring the Y_n lines of the tag CAM, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).