



## 8080A-2

# SINGLE CHIP 8-BIT N-CANNEL MICROPROCESSOR

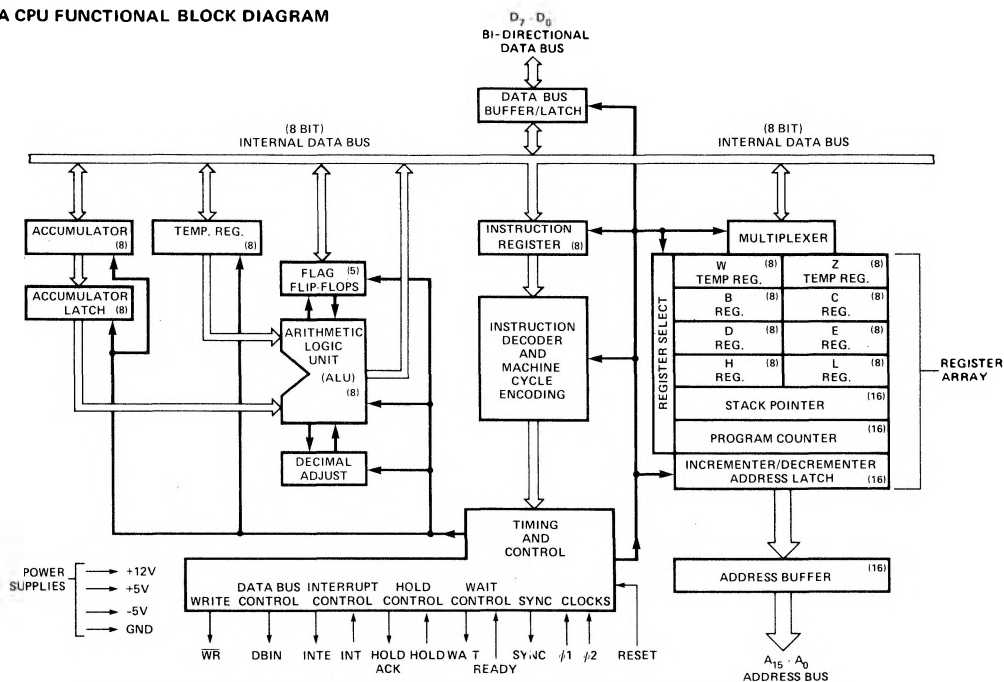
- TTL Drive Capability
- 1.5  $\mu$ s Instruction Cycle
- Powerful Problem Solving Instruction Set
- Six General Purpose Registers and an Accumulator
- Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory
- Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment
- Decimal, Binary and Double Precision Arithmetic
- Ability to Provide Priority Vectored Interrupts
- 512 Directly Addressed I/O Ports

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications. The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR'ing these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS\***

|   |                 |
|---|-----------------|
| Temperature Under Bias                                    | 0°C to +70°C    |
| Storage Temperature                                       | -65°C to +150°C |
| All Input or Output Voltages                              |                 |
| With Respect to $V_{BB}$                                  | -0.3V to +20V   |
| $V_{CC}$ , $V_{DD}$ and $V_{SS}$ With Respect to $V_{BB}$ | -0.3V to +20V   |
| Power Dissipation   | 1.5W            |

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = +12\text{V} \pm 5\%$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ , Unless Otherwise Noted.

| Symbol              | Parameter                                | Min.       | Typ. | Max.         | Unit                | Test Condition   |
|---------------------|--|------------|------|--------------|---------------------|--|
| $V_{ILC}$           | Clock Input Low Voltage                  | $V_{SS}-1$ |      | $V_{SS}+0.8$ | V                   |  |
| $V_{IHC}$           | Clock Input High Voltage                 | 9.0        |      | $V_{DD}+1$   | V                   |  |
| $V_{IL}$            | Input Low Voltage                        | $V_{SS}-1$ |      | $V_{SS}+0.8$ | V                   |  |
| $V_{IH}$            | Input High Voltage                       | 3.3        |      | $V_{CC}+1$   | V                   |  |
| $V_{OL}$            | Output Low Voltage                       |            |      | 0.45         | V                   | $I_{OL} = 1.9\text{mA}$ on all outputs,<br>$I_{OH} = 150\mu\text{A}$ .                           |
| $V_{OH}$            | Output High Voltage                      | 3.7        |      |              | V                   |  |
| $I_{DD}(\text{AV})$ | Avg. Power Supply Current ( $V_{DD}$ )   |            | 40   | 70           | mA                  | Operation<br>$T_{CY} = .38\mu\text{sec}$   |
| $I_{CC}(\text{AV})$ | Avg. Power Supply Current ( $V_{CC}$ )   |            | 60   | 80           | mA                  |  |
| $I_{BB}(\text{AV})$ | Avg. Power Supply Current ( $V_{BB}$ )   |            | .01  | 1            | mA                  |  |
| $I_{IL}$            | Input Leakage                            |            |      | $\pm 10$     | $\mu\text{A}$       | $V_{SS} \leq V_{IN} \leq V_{CC}$   |
| $I_{CL}$            | Clock Leakage                            |            |      | $\pm 10$     | $\mu\text{A}$       | $V_{SS} \leq V_{CLOCK} \leq V_{DD}$  |
| $I_{DL}^{[2]}$      | Data Bus Leakage in Input Mode           |            |      | -100<br>-2.0 | $\mu\text{A}$<br>mA | $V_{SS} \leq V_{IN} \leq V_{SS} + 0.8\text{V}$<br>$V_{SS} + 0.8\text{V} \leq V_{IN} \leq V_{CC}$ |
| $I_{FL}$            | Address and Data Bus Leakage During HOLD |            |      | +10<br>-100  | $\mu\text{A}$       | $V_{ADDR/DATA} = V_{CC}$<br>$V_{ADDR/DATA} = V_{SS} + 0.45\text{V}$                              |

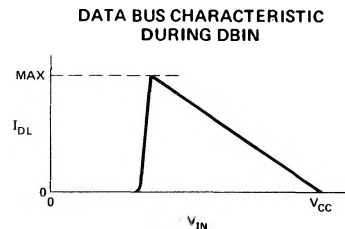
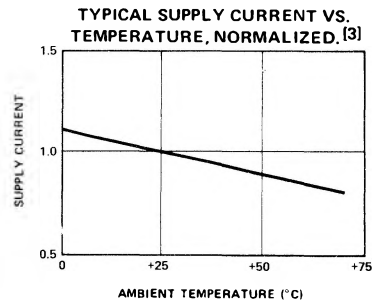
**CAPACITANCE**

$T_A = 25^\circ\text{C}$   $V_{CC} = V_{DD} = V_{SS} = 0\text{V}$ ,  $V_{BB} = -5\text{V}$

| Symbol    | Parameter          | Typ. | Max. | Unit | Test Condition   |
|-----------|--------------------|------|------|------|--|
| $C_\phi$  | Clock Capacitance  | 17   | 25   | pf   | $f_c = 1\text{MHz}$<br>Unmeasured Pins<br>Returned to $V_{SS}$ |
| $C_{IN}$  | Input Capacitance  | 6    | 10   | pf   |  |
| $C_{OUT}$ | Output Capacitance | 10   | 20   | pf   |  |

**NOTES:**

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and  $V_{IN} > V_{IH}$  an internal active pull up will be switched onto the Data Bus.
3.  $\Delta I_{supply} / \Delta T_A = -0.45\%/^\circ\text{C}$ .

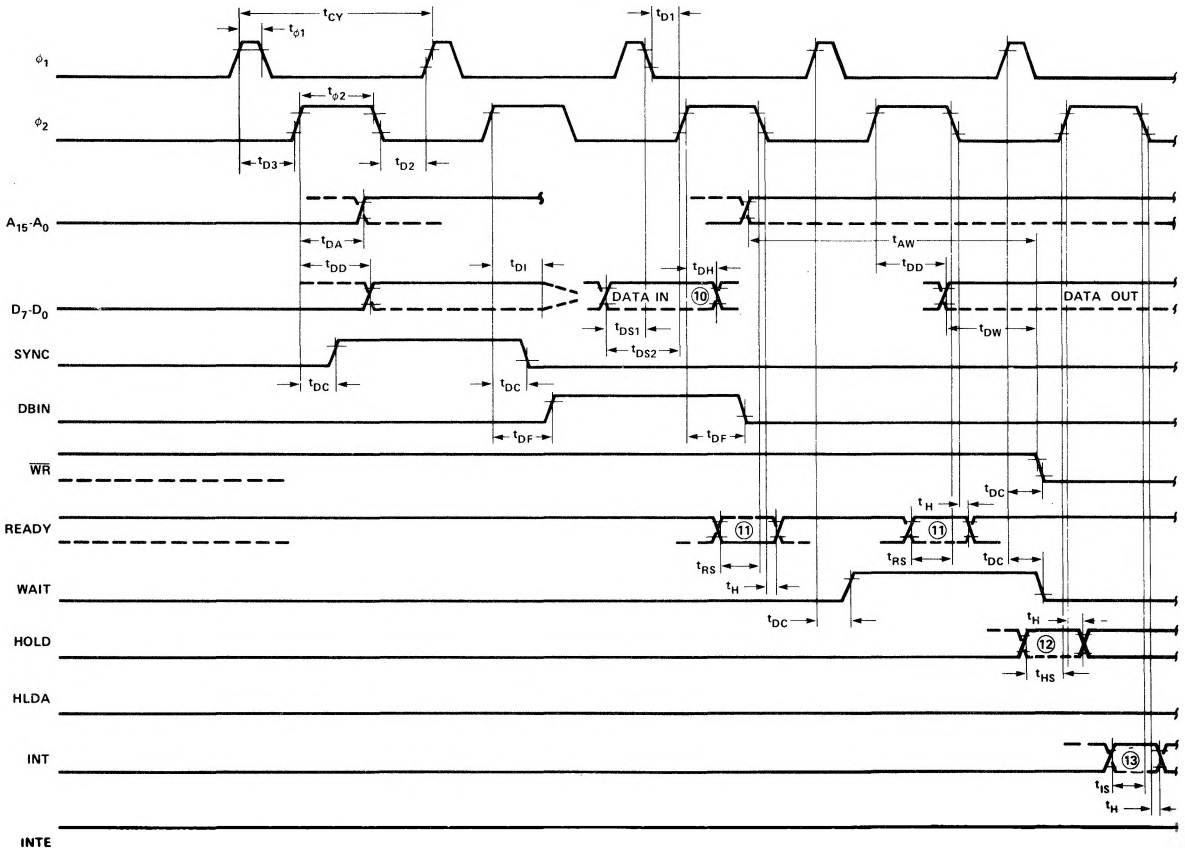


**A.C. CHARACTERISTICS**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = +12\text{V} \pm 5\%$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ , Unless Otherwise Noted

| Symbol         | Parameter  | Min. | Max.     | Unit            | Test Condition                              |
|----------------|--|------|----------|-----------------|---|
| $t_{CY}^{[3]}$ | Clock Period   | .38  | 2.0      | $\mu\text{sec}$ | $C_L = 100\text{pf}$<br>$C_L = 50\text{pf}$ |
| $t_r, t_f$     | Clock Rise and Fall Time   | 0    | 50       | nsec            |   |
| $t_{\phi 1}$   | $\phi_1$ Pulse Width   | 60   |          | nsec            |   |
| $t_{\phi 2}$   | $\phi_2$ Pulse Width   | 175  |          | nsec            |   |
| $t_{D1}$       | Delay $\phi_1$ to $\phi_2$   | 0    |          | nsec            |   |
| $t_{D2}$       | Delay $\phi_2$ to $\phi_1$   | 70   |          | nsec            |   |
| $t_{D3}$       | Delay $\phi_1$ to $\phi_2$ Leading Edges   | 70   |          | nsec            |   |
| $t_{DA}^{[2]}$ | Address Output Delay From $\phi_2$   |      | 175      | nsec            |   |
| $t_{DD}^{[2]}$ | Data Output Delay From $\phi_2$  |      | 200      | nsec            |   |
| $t_{DC}^{[2]}$ | Signal Output Delay From $\phi_1$ , or $\phi_2$ (SYNC, $\overline{WR}$ , WAIT, HLDA) |      | 120      | nsec            |   |
| $t_{DF}^{[2]}$ | DBIN Delay From $\phi_2$   | 25   | 140      | nsec            |   |
| $t_{DI}^{[1]}$ | Delay for Input Bus to Enter Input Mode  |      | $t_{DF}$ | nsec            |   |
| $t_{DS1}$      | Data Setup Time During $\phi_1$ and DBIN   | 20   |          | nsec            |   |

**TIMING WAVEFORMS<sup>[14]</sup>** (Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



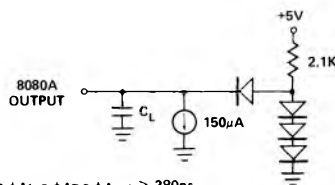
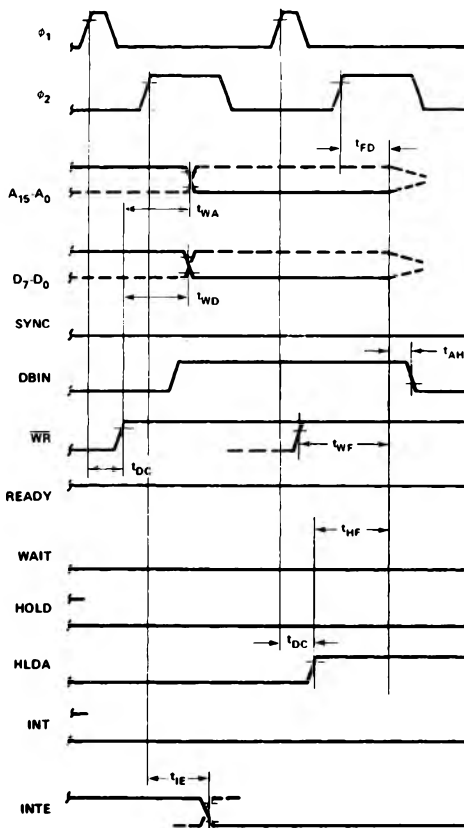
**A.C. CHARACTERISTICS** (Continued)

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = +12\text{V} \pm 5\%$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ , Unless Otherwise Noted

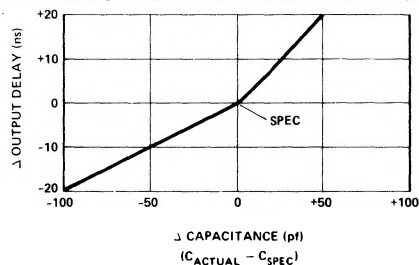
| Symbol         | Parameter   | Min. | Max. | Unit | Test Condition   |
|----------------|---|------|------|------|--|
| $t_{DS2}$      | Data Setup Time to $\phi_2$ During DBIN                       | 130  |      | nsec | $C_L = 50\text{pf}$  |
| $t_{DH}^{[1]}$ | Data Hold Time From $\phi_2$ During DBIN                      | [1]  |      | nsec |  |
| $t_{IE}^{[2]}$ | INTE Output Delay From $\phi_2$                               |      | 200  | nsec |  |
| $t_{RS}$       | READY Setup Time During $\phi_2$                              | 90   |      | nsec |  |
| $t_{HS}$       | HOLD Setup Time to $\phi_2$                                   | 120  |      | nsec |  |
| $t_{IS}$       | INT Setup Time During $\phi_2$ (During $\phi_1$ in Halt Mode) | 100  |      | nsec | $C_L = 100\text{pf}$ : Address, Data<br>$C_L = 50\text{pf}$ : WR, HLDA, DBIN |
| $t_H$          | Hold Time From $\phi_2$ (READY, INT, HOLD)                    | 0    |      | nsec |  |
| $t_{FD}$       | Delay to Float During Hold (Address and Data Bus)             |      | 120  | nsec |  |
| $t_{AW}^{[2]}$ | Address Stable Prior to WR                                    | [5]  |      | nsec |  |
| $t_{DW}^{[2]}$ | Output Data Stable Prior to WR                                | [6]  |      | nsec |  |
| $t_{WD}^{[2]}$ | Output Data Stable From WR                                    | [7]  |      | nsec |  |
| $t_{WA}^{[2]}$ | Address Stable From WR  | [7]  |      | nsec |  |
| $t_{HF}^{[2]}$ | HLDA to Float Delay   | [8]  |      | nsec |  |
| $t_{WF}^{[2]}$ | WR to Float Delay   | [9]  |      | nsec |  |
| $t_{AH}^{[2]}$ | Address Hold Time After DBIN During HLDA                      | -20  |      | nsec |  |

## NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured.  $t_{DH} = 50\text{ ns}$  or  $t_{DF}$ , whichever is less.
2. Load Circuit.



$$3. \quad t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1} \geq 380\text{ns.}$$

TYPICAL  $\Delta$  OUTPUT DELAY VS.  $\Delta$  CAPACITANCE

4. The following are relevant when interfacing the 8080A to devices having  $V_{IH} = 3.3\text{V}$ :
  - a) Maximum output rise time from .8V to 3.3V = 100ns @  $C_L = \text{SPEC}$ .
  - b) Output delay when measured to 3.0V = SPEC + 60ns @  $C_L = \text{SPEC}$ .
  - c) If  $C_L \neq \text{SPEC}$ , add .6ns/pf if  $C_L > C_{\text{SPEC}}$ , subtract .3ns/pf (from modified delay) if  $C_L < C_{\text{SPEC}}$ .
5.  $t_{AW} = 2 t_{CY} - t_{D3} - t_{r\phi 2} - 130\text{nsec}$ .
6.  $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - 170\text{nsec}$ .
7. If not HLDA,  $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10\text{ns}$ . If HLDA,  $t_{WD} = t_{WA} = t_{WF}$ .
8.  $t_{HF} = t_{D3} + t_{r\phi 2} - 50\text{ns}$ .
9.  $t_{WF} = t_{D3} + t_{r\phi 2} - 10\text{ns}$ .
10. Data in must be stable for this period during DBIN  $\cdot T_3$ . Both  $t_{DS1}$  and  $t_{DS2}$  must be satisfied.
11. Ready signal must be stable for this period during  $T_2$  or  $T_W$ . (Must be externally synchronized.)
12. Hold signal must be stable for this period during  $T_2$  or  $T_W$  when entering hold mode, and during  $T_3$ ,  $T_4$ ,  $T_5$  and  $T_{WH}$  when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.