National Semiconductor

74LVQ374
Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

General Description

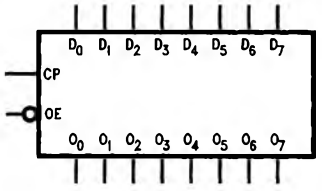
The LVQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- MIL-STD-883 54ACQ Products are available for Military/Aerospace Applications

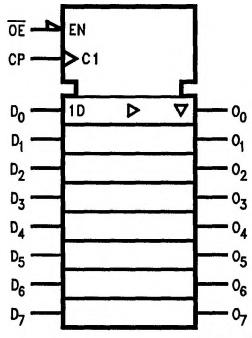
Ordering Code: See Section 11

Logic Symbols



TL/F/11360–1

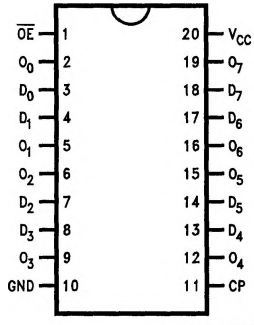
IEEE/IEC



TL/F/11360–2

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11360–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SOIC JEDEC
Order Number	74LVQ374SC 74LVQ374SCX	74LVQ374SJ 74LVQ374SJX	74LVQ374QSC 74LVQ374QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

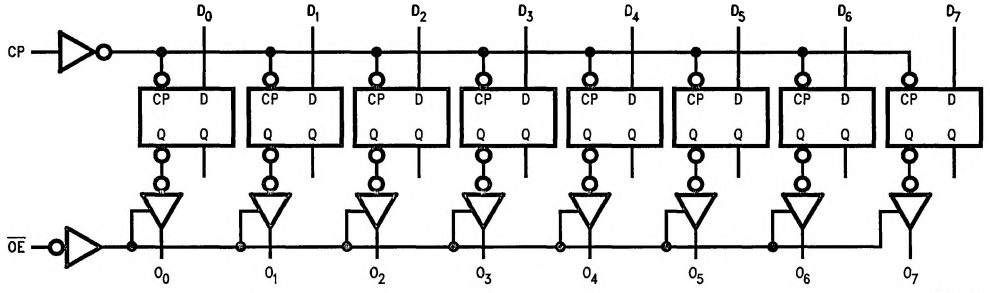
The LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



TL/F/11360–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ374 T_A = +25°C		74LVQ374 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ374 $T_A = +25°C$ Typ	74LVQ374 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6		−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6	4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum TRI-STATE Leakage Current	3.6	±0.25	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8	V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ374 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ374 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	55 75			50 70		MHz
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	2.7 3.3 ±0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t_{PZL}, t_{PZH}	Output Enable Time	2.7 3.3 ±0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0 1.0	11.4 9.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew* CP to O_n	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ374 $T_A = +25°C$, $C_L = 50$ pF		74LVQ374 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	0 0	4.0 3.0	4.5 3.0	ns
t_H	Hold Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3	0 0	1.5 1.5	1.5 1.5	ns
t_W	CP Pulse Width, HIGH or LOW	2.7 3.3 ±0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	39	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.