Rambus® 64 Bit RIMM™ Module (with 256/288Mb RDRAM Devices)

Overview

The Rambus® 64 Bit RIMM™ module is a general purpose high-performance line of memory modules suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The Rambus 64 Bit RIMM module consists of 256Mb / 288Mb RDRAM® devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits the use of conventional system and board design technologies. RIMM 6400 modules support 800MHz transfer rates. RIMM 8500 modules support 1066MHz transfer rates.

The 64 Bit RIMM module provides four 16 or 18 bit memory channels to faciliate compact system design. Channels B and D enter and exit the module to support connections to or from a controller, memory slot, or termination. Channels A and C are terminated on the module and support a connection from a controller or another memory slot.

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM device multi-bank architecture supports up to four simultaneous transactions per device.

Related Documentation

Data sheets for Rambus memory system components, including the RDRAM device, RIMM modules, and RIMM connectors are available on the Rambus web site at http://www.rambus.com.

Features

- 4 RDRAM channels, 2 pass through and 2 terminated on 64 Bit RIMM module
- High speed 800 and 1066 MHz RDRAM devices
- 326 edge connector pads with 0.76mm pad spacing
- Module PCB size: 133.35mm x 34.93mm x 1.27mm (5.25” x 1.375” x 0.05”)
- Gold plated edge connector pad contacts
- Serial Presence Detect (SPD) support
- Operates from a 1.8 volt supply (±5%)
- Low power and powerdown self refresh modes
- Separate Row and Column buses for higher efficiency, Row and Column busses shared across 4 channels on module

Key Timing Parameters

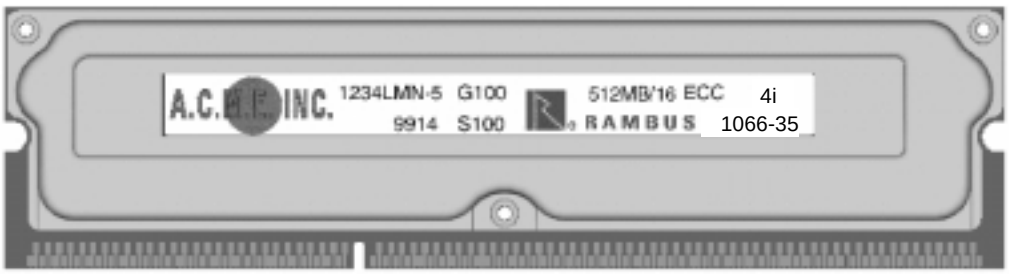
The following table lists the frequency and latency bins available for 64 Bit RIMM modules.

Table 1: RIMM Module Frequency and Latency

RDRAM Core Organization	I/O Freq. MHz	t_{rac} (Core Access Time) ns
x 16	800	45
x 16	800	40
x 16	1066	35
x 18	800	45
x18	800	40
x18	1066	35

Form Factor

The Rambus 64 Bit RIMM modules are offered in 326 pad 0.76 mm edge connector pad pitch suitable for 326 contact RIMM connectors.



Rambus 64 Bit RIMM module with heat spreader

Table 2: Module Pad Number and Signal Names

Pad	Signal Name	Pad	Signal Name
A1	Gnd	B1	Gnd
A2	ADQA8_L	B2	ADQA7_L
A3	Gnd	B3	Gnd
A4	ADQA6_L	B4	ADQA5_L
A5	Gnd	B5	Gnd
A6	ADQA4_L	B6	ADQA3_L
A7	Gnd	B7	Gnd
A8	ADQA2_L	B8	ADQA1_L
A9	Gnd	B9	Gnd
A10	ADQA0_L	B10	ACTMN_L
A11	Gnd	B11	Gnd
A12	ACTM_L	B12	ADQB0_L
A13	Gnd	B13	Gnd
A14	ADQB1_L	B14	ADQB2_L
A15	Gnd	B15	Gnd
A16	ADQB3_L	B16	ADQB4_L
A17	Gnd	B17	Gnd
A18	ADQB5_L	B18	ADQB6_L
A19	Gnd	B19	Gnd
A20	ADQB7_L	B20	ADQB8_L
A21	Gnd	B21	Gnd
A22	ACTM_R	B22	ACTMN_R
A23	Gnd	B23	Gnd
A24	BDQA8_L	B24	BDQA7_L
A25	Gnd	B25	Gnd
A26	BDQA6_L	B26	BDQA5_L
A27	Gnd	B27	Gnd
A28	BDQA4_L	B28	BDQA3_L
A29	Gnd	B29	Gnd
A30	BDQA2_L	B30	BDQA1_L
A31	Gnd	B31	Gnd
A32	BDQA0_L	B32	BCTMN_L
A33	Gnd	B33	Gnd
A34	BCTM_L	B34	BDQB0_L
A35	Gnd	B35	Gnd
A36	BDQB1_L	B36	BDQB2_L
A37	Gnd	B37	Gnd
A38	BDQB3_L	B38	BDQB4_L
A39	Gnd	B39	Gnd
A40	BDQB5_L	B40	BDQB6_L
A41	Gnd	B41	Gnd
A42	BDQB7_L	B42	BDQB8_L
A43	Gnd	B43	Gnd
A44	CMD	B44	SCK
A45	Gnd	B45	Gnd
A46	CFM	B46	CFMN

Pad	Signal Name	Pad	Signal Name
A82	Vterm	B82	Vterm
A83	Gnd	B83	Gnd
A84	CDQA8_L	B84	CDQA7_L
A85	Gnd	B85	Gnd
A86	CDQA6_L	B86	CDQA5_L
A87	Gnd	B87	Gnd
A88	CDQA4_L	B88	CDQA3_L
A89	Gnd	B89	Gnd
A90	CDQA2_L	B90	CDQA1_L
A91	Gnd	B91	Gnd
A92	CDQA0_L	B92	CCTMN_L
A93	Gnd	B93	Gnd
A94	CCTM_L	B94	CDQB0_L
A95	Gnd	B95	Gnd
A96	CDQB1_L	B96	CDQB2_L
A97	Gnd	B97	Gnd
A98	CDQB3_L	B98	CDQB4_L
A99	Gnd	B99	Gnd
A100	CDQB5_L	B100	CDQB6_L
A101	Gnd	B101	Gnd
A102	CDQB7_L	B102	CDQB8_L
A103	Gnd	B103	Gnd
A104	V_{CMOS}	B104	V_{CMOS}
A105	Gnd	B105	Gnd
A106	Vref	B106	Vref
A107	Gnd	B107	Gnd
A108	Vdd	B108	Vdd
A109	Vdd	B109	Vdd
A110	Vdd	B110	Vdd
A111	Gnd	B111	Gnd
A112	Vdd	B112	Vdd
A113	Gnd	B113	Gnd
A114	Vdd	B114	Vdd
A115	Vdd	B115	Vdd
A116	SA2	B116	SA1
A117	Gnd	B117	Gnd
A118	SA0	B118	SWP
A119	SVdd	B119	SVdd
A120	SCL	B120	SDA
A121	Gnd	B121	Gnd
A122	CCTM_R	B122	CCTMN_R
A123	Gnd	B123	Gnd
A124	DDQA8_L	B124	DDQA7_L
A125	Gnd	B125	Gnd
A126	DDQA6_L	B126	DDQA5_L
A127	Gnd	B127	Gnd

Table 2: Module Pad Number and Signal Names

Pad	Signal Name	Pad	Signal Name
A47	Gnd	B47	Gnd
A48	ROW2	B48	ROW1
A49	Gnd	B49	Gnd
A50	ROW0	B50	COL4
A51	Gnd	B51	Gnd
A52	COL3	B52	COL2
A53	Gnd	B53	Gnd
A54	COL1	B54	COL0
A55	Gnd	B55	Gnd
A56	SIN	B56	SOUT
A57	Gnd	B57	Gnd
A58	BDQB8_R	B58	BDQB7_R
A59	Gnd	B59	Gnd
A60	BDQB6_R	B60	BDQB5_R
A61	Gnd	B61	Gnd
A62	BDQB4_R	B62	BDQB3_R
A63	Gnd	B63	Gnd
A64	BDQB2_R	B64	BDQB1_R
A65	Gnd	B65	Gnd
A66	BDQB0_R	B66	BCTM_R
A67	Gnd	B67	Gnd
A68	BCTMN_R	B68	BDQA0_R
A69	Gnd	B69	Gnd
A70	BDQA1_R	B70	BDQA2_R
A71	Gnd	B71	Gnd
A72	BDQA3_R	B72	BDQA4_R
A73	Gnd	B73	Gnd
A74	BDQA5_R	B74	BDQA6_R
A75	Gnd	B75	Gnd
A76	BDQA7_R	B76	BDQA8_R
A77	Gnd	B77	Gnd
A78	Vterm	B78	Vterm
A79	Vterm	B79	Vterm
A80	Vterm	B80	Vterm
A81	Vterm	B81	Vterm

Pad	Signal Name	Pad	Signal Name
A128	DDQA4_L	B128	DDQA3_L
A129	Gnd	B129	Gnd
A130	DDQA2_L	B130	DDQA1_L
A131	Gnd	B131	Gnd
A132	DDQA0_L	B132	DCTMN_L
A133	Gnd	B133	Gnd
A134	DCTM_L	B134	DDQB0_L
A135	Gnd	B135	Gnd
A136	DDQB1_L	B136	DDQB2_L
A137	Gnd	B137	Gnd
A138	DDQB3_L	B138	DDQB4_L
A139	Gnd	B139	Gnd
A140	DDQB5_L	B140	DDQB6_L
A141	Gnd	B141	Gnd
A142	DDQB7_L	B142	DDQB8_L
A143	Gnd	B143	Gnd
A144	DDQB8_R	B144	DDQB7_R
A145	Gnd	B145	Gnd
A146	DDQB6_R	B146	DDQB5_R
A147	Gnd	B147	Gnd
A148	DDQB4_R	B148	DDQB3_R
A149	Gnd	B149	Gnd
A150	DDQB2_R	B150	DDQB1_R
A151	Gnd	B151	Gnd
A152	DDQB0_R	B152	DCTM_R
A153	Gnd	B153	Gnd
A154	DCTMN_R	B154	DDQA0_R
A155	Gnd	B155	Gnd
A156	DDQA1_R	B156	DDQA2_R
A157	Gnd	B157	Gnd
A158	DDQA3_R	B158	DDQA4_R
A159	Gnd	B159	Gnd
A160	DDQA5_R	B160	DDQA6_R
A161	Gnd	B161	Gnd
A162	DDQA7_R	B162	DDQA8_R
A163	Gnd	B163	Gnd

Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
ACTM_L	A12	**O**	**RSL**	Channel A clock to master. Interface clock used for transmitting RSL signals to Channel A. Positive polarity. Connects to left RDRAM device on Channel A.
ACTM_R	A22	**O**	**RSL**	Channel A clock to master. Interface clock used for transmitting RSL signals to Channel A. Positive polarity. Connects to right RDRAM device on Channel A.
ACTMN_L	B10	**O**	**RSL**	Channel A clock to master. Interface clock used for transmitting RSL signals to Channel A. Negative polarity. Connects to left RDRAM device on Channel A
ACTMN_R	B22	**O**	**RSL**	Channel A clock to master. Interface clock used for transmitting RSL signals to Channel A. Negative polarity. Connects to right RDRAM device on Channel A
ADQA8_L.. ADQA0_L	A2, B2, A4, B4, A6, B6, A8, B8, A10	**I/O**	**RSL**	Channel A Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel A. ADQA8_L is non-functional on modules with x16 RDRAM devices
ADQB8_L.. ADQB0_L	B20, A20, B18, A18, B16, A16, B14, A14, B12	**I/O**	**RSL**	Channel A Data bus B. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel A. ADQB8_L is non-functional on modules with x16 RDRAM devices
BCTM_L	A34	**O**	**RSL**	Channel B clock to master. Interface clock used for transmitting RSL signals to Channel B. Positive polarity. Connects to left RDRAM device on Channel B
BCTM_R	B66	**O**	**RSL**	Channel B Clock to master. Interface clock used for transmitting RSL signals to Channel B. Positive polarity. Connects to right RDRAM device on Channel B
BCTMN_L	B32	**O**	**RSL**	Channel B clock to master. Interface clock used for transmitting RSL signals to Channel B. Negative polarity. Connects to left RDRAM device on Channel B.
BCTMN_R	B68	**O**	**RSL**	Channel B Clock to master. Interface clock used for transmitting RSL signals to Channel B. Negative polarity. Connects to right RDRAM device on Channel B
BDQA8_L.. BDQA0_L	A24, B24, A26, B26, A28, B28, A30, B30, A32	**I/O**	**RSL**	Channel B Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel B. BDQA8_L is non-functional on modules with x16 RDRAM devices
BDQB8_L.. BDQB0_L	B42, A42, B40, A40, B38, A38, B36, A36, B34	**I/O**	**RSL**	Channel B Data bus B. A 9-bit bus carrying a byte of read or write data between Channel B and the left RDRAM device on Channel B. BDQB8_L is non-functional on modules with x16 RDRAM devices.
BDQA8_R.. BDQA0_R	B76, A76, B74, A74, B72, A72, B70, A70, B68	**I/O**	**RSL**	Channel B Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the right RDRAM device on Channel B. BDQA8_R is non-functional on modules with x16 RDRAM devices.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
BDQB8_R.. BDQB0_R	A58, B58, A60, B60, A62, B62, A64, B64, A66	**I/O**	**RSL**	Channel B Data bus B. A 9-bit bus carrying a byte of read or write data between Channel and the right RDRAM device on Channel B. BDQB8_R is non-functional on modules with x16 RDRAM devices.
CCTM_L	A94	**O**	**RSL**	Channel C clock to master. Interface clock used for transmitting RSL signals to Channel C. Positive polarity. Connects to left RDRAM device on Channel C
CCTM_R	A122	**O**	**RSL**	Channel C clock to master. Interface clock used for transmitting RSL signals to Channel C. Positive polarity. Connects to right RDRAM device on Channel C
CCTMN_L	B92	**O**	**RSL**	Channel C clock to master. Interface clock used for transmitting RSL signals to Channel C. Negative polarity. Connects to left RDRAM device on Channel C
CCTMN_R	B122	**O**	**RSL**	Channel C clock to master. Interface clock used for transmitting RSL signals to Channel C. Negative polarity. Connects to right RDRAM device on Channel C
CDQA8_L.. CDQA0_L	A84, B84, A86, B86, A88, B88, A90, B90, A92	**I/O**	**RSL**	Channel C Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel C. CDQA8_L is non-functional on modules with x16 RDRAM devices
CDQB8_L.. CDQB0_L	B102, A102, B100, A100, B98, A98, B96, A96, B94	**I/O**	**RSL**	Channel C Data bus B. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel C. CDQB8_L is non-functional on modules with x16 RDRAM devices.
CFM	A46	**I**	**RSL**	Clock From Master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	B46	**I**	**RSL**	Clock From Master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CMD	A44	**I**	**V_{CMOS}**	Serial Command used to read from and write to the control registers. Also used for power management.
COL4.. COL0	B50, A52, B52, A54, B54	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.
DCTM_L	A134	**O**	**RSL**	Channel D clock to master. Interface clock used for transmitting RSL signals to Channel D. Positive polarity. Connects to left RDRAM device on Channel D
DCTM_R	B152	**O**	**RSL**	Channel D clock to master. Interface clock used for transmitting RSL signals to Channel D. Positive polarity. Connects to right RDRAM device on Channel D
DCTMN_L	B132	**O**	**RSL**	Channel D clock to master. Interface clock used for transmitting RSL signals to Channel D. Negative polarity. Connects to left RDRAM device on Channel D.
DCTMN_R	A154	**O**	**RSL**	Channel D clock to master. Interface clock used for transmitting RSL signals to Channel D. Negative polarity. Connects to right RDRAM device on Channel D.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
DDQA8_L.. DDQA0_L	A124, B124, A126, B126, A128, B128, A130, B130, A132	I/O	RSL	Channel D Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel D. DDQA8_L is non-functional on modules with x16 RDRAM devices
DDQA8_R.. DDQA0_R	B162, A162, B160, A160, B158, A158, B156, A156, B154	I/O	RSL	Channel D Data bus A. A 9-bit bus carrying a byte of read or write data between Channel and the right RDRAM device on Channel D. DDQA8_R is non-functional on modules with x16 RDRAM devices.
DDQB8_L.. DDQB0_L	B142, A142, B140, A140, B138, A138, B136, A136, B134	I/O	RSL	Channel D Data bus B. A 9-bit bus carrying a byte of read or write data between Channel and the left RDRAM device on Channel D. DDQB8_L is non-functional on modules with x16 RDRAM devices.
DDQB8_R.. DDQB0_R	A144, B144, A146, B146, A148, B148, A150, B150, A152	I/O	RSL	Channel D Data bus B. A 9-bit bus carrying a byte of read or write data between Channel and the right RDRAM device on Channel D. DDQB8_R is non-functional on modules with x16 RDRAM devices.
Gnd	A1 A3 A5 A7 A9 A11 A13 A15 A17 A19 A21 A23 A25 A27 A29 A31 A33 A35 A37 A39 A41 A43 A45 A47 A49 A51 A53 A55 A57 A59 A61 A63 A65 A67 A69 A71 A73 A75 A77 A83 A85 A87 A89 A91 A93 A95 A97 A99 A101 A103 A105 A107 A111 A113 A117 A121 A123 A125 A127 A129 A131 A133 A135 A137 A139 A141 A143 A145 A147 A149 A151 A153 A155 A157 A159 A161 A163 B1 B3 B5 B7 B9 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B35 B37 B39 B41 B43 B45 B47 B49 B51 B53 B55 B57 B59 B61 B63 B65 B67 B69 B71 B73 B75 B77 B83 B85 B87 B89 B91 B93 B95 B97 B99 B101 B103 B105 B107 B111 B113 B117 B121 B123 B125 B127 B129 B131 B133 B135 B137 B139 B141 B143 B145 B147 B149 B151 B153 B155 B157 B159 B161 B163			Ground reference for RDRAM device core and interface.
ROW2.. ROW0	A48, B48, A50	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses to Channels.
SA0	A118	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B116	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	A116	I	SV_{DD}	Serial Presence Detect Address 2.
SCK	B44	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the Channel RDRAM device control registers.

Table 3: Module Connector Pad Description (Continued)

Signal	Module Connector Pads	I/O	Type	Description
SCL	A120	**I**	**SV_{DD}**	Serial Presence Detect Clock.
SDA	B120	**I/O**	**SV_{DD}**	Serial Presence Detect Data (Open Collector I/O).
SIN	A56	**I/O**	**V_{CMOS}**	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the left RDRAM device on Channel A.
SOUT	B56	**I/O**	**V_{CMOS}**	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the right RDRAM device on Channel D.
SV_{DD}	A119, B119			SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.
SWP	B118	**I**	**SV_{DD}**	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A104, B104			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A108, B108, A109, B109, A110, B110, A112, B112, A114, B114, A115, B115			Supply voltage for the RDRAM device core and interface logic.
Vref	A106, B106			Logic threshold reference voltage for RSL signals.
Vterm	A78, B78, A79, B79, A80, B80, A81, B81, A82, B82			Termination voltage

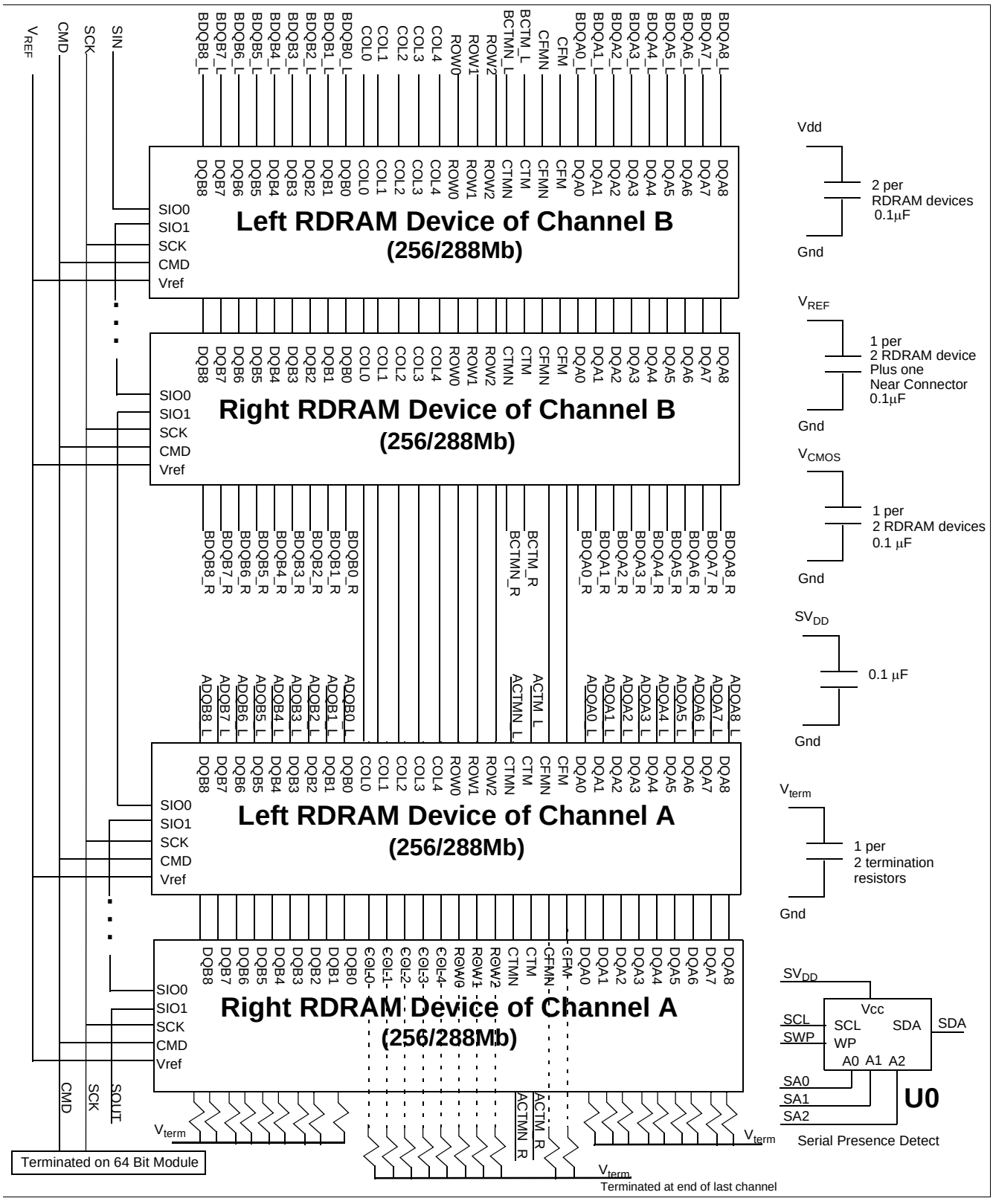


Figure 1: 64 Bit RIMM Module Functional Diagram Shows Two of the Four Channels

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C

DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage[a]	1.80 - 0.09	1.80 + 0.09	V
V_{CMOS}	CMOS I/O power supply at pad for 1.8V controllers	V_{DD}	V_{DD}	V
V_{REF}	Reference voltage[a]	1.4 - 0.2	1.4 + 0.2	V
V_{SPD}	Serial Presence Detector- positive power supply	2.2	3.6	V
V_{TERM}	Termination voltage	1.80 - 0.09	1.80 + 0.09	V

a. see RDRAM device datasheet for more details

AC Electrical Specifications

Symbol	Parameter and Conditions:[a] 128MB, 256MB, 512MB Modules	Min	Typ	Max	Unit
Z_L	Module impedance of RSL signals	36.0	40.0	44.0	Ω
$Z_{UL\text{-}CMOS}$	Module impedance of SCK and CMD signals	34.0	40.0	46.0	Ω
T_{PD}	Average clock delay from finger to termination of RSL clock nets CTM and CTMN	-		1560[b]	ps
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} [a,c]	-21		21	ps
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK signal with respect to an average clock delay [a]	-250		250	ps
$\Delta T_{PD\text{-}SCK,CMD}$	Propagation delay variation of CMD signal with respect to SCK signal	-200		200	ps
V_α / V_{IN}	Attenuation limit			16.0	%
V_{XF} / V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)			4.0	%
V_{XB} / V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)			2.0	%
R_{DC}	DC resistance limit	-	-	0.8	Ω

a. Specifications apply per channel
b. T_{PD} or Average clock delay is defined as the average delay from finger to termination of CTM RSL clock nets (CTM and CTMN). Specification applies per channel.
c. If the 64 Bit RIMM module meets the following specification, it is compliant to the specification. If the 64 Bit RIMM module does not meet these specifications, the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table.

Adjusted ΔT_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min / Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 4, 8, and 16 device modules	+/-[17+(18*(N/4)*ΔZ0)][a]	-30	30	ps

a. Where: N = Number of RDRAM devices installed on the RIMM module
ΔZ0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

Physical Dimensions

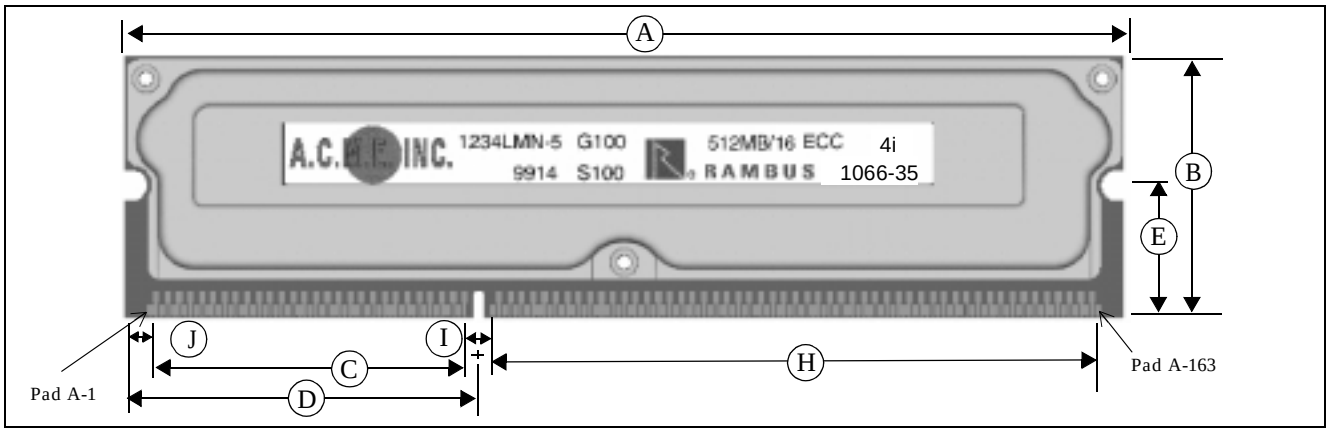


Table 4: 64 Bit RIMM Module PCB Physical Description

Dimension	Description	Min	Nom	Max	Unit
A	PCB length	133.20 5.244	133.35 5.250	133.50 5.256	mm in
B	PCB height for 1.375” RIMM Module		34.93 1.375	35.08 1.381	mm in
C	Center-center pad width from pad A1 to A56 B1 to B56		41.910 1.649		mm in
D	Spacing from PCB left edge to connector key notch		47.240 1.858		mm in
E	Spacing from contact pad PCB edge to side edge retainer notch			17.78 0.700	mm in
F	PCB thickness	1.17 0.046	1.27 0.050	1.37 0.054	mm in
G	Heat spreader thickness from PCB surface (one side) to heat spreader top surface			3.00 0.118	mm in
H	Center-center pad width from pad A57 to A163, B57 to B163		80.772 3.177		mm in
I	Center-center pad width from pad A56 to A57, B56 to B57		3.810 0.150		mm in
J	Spacing from PCB left edge to center of pad A1, B1		3.429 0.135		mm in

Serial Presence Detect

The 64 Bit RIMM module supports the use of a Serial Presence Detect EEPROM. The specification and definition of the contents of this function are documented in the Serial Presence Detect Specification (DL-0066).

Module Weight

The maximum 64 Bit RIMM module weight is 45 gm (1.575 oz) with a center of mass 35mm (1.378 in.) upwards from bottom edge.

Standard RIMM Module Marking

The 64 Bit RIMM modules available from RIMM module manufacturers will be marked as shown. This industry standard marking will help OEMs and users identify the Rambus RIMM modules for use in specific system applications. This marking also assists OEMs or users to specify and verify if the correct RIMM modules are installed in their systems. In the diagram, a label is shown attached to the RIMM module's heat spreader. This label contains suggested vendor specific information. Information contained on the label is specific to the RIMM module and provides RDRAM information without requiring removal of the 32 Bit RIMM module's heat spreader.

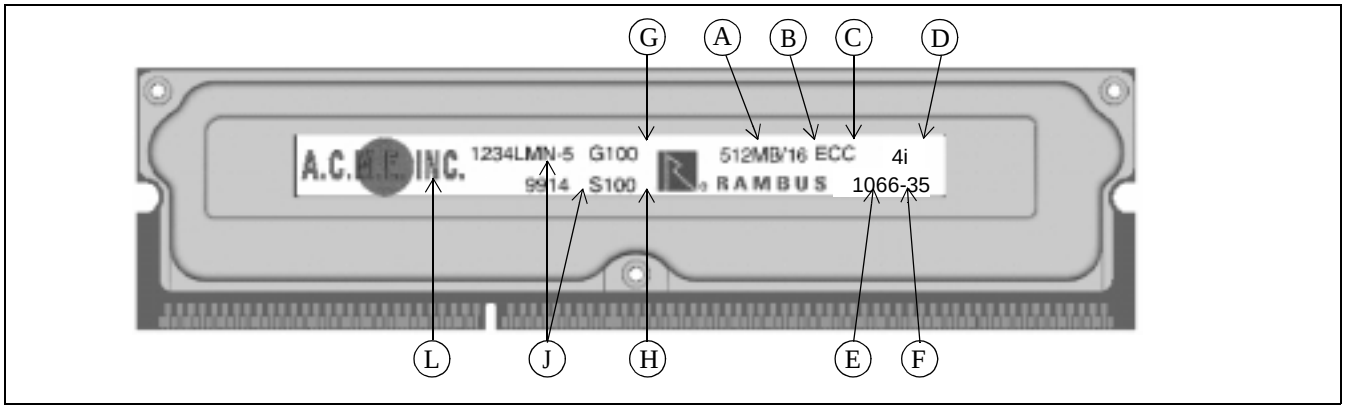


Table 5: Standard 64 Bit RIMM Module Marking

	Label Field	Description	Marked Text	Unit
A	Module Memory Capacity	Total Number of 8-bit or 9-bit MBytes of RDRAM device storage in RIMM module	512MB, 256MB, 128MB	MBytes
B	Number of RDRAMs	Total number of RDRAM devices contained in the RIMM module	/16, /8, /4	RDRAM devices
C	ECC Support	Indicates whether the RIMM module supports 8-bit (no ECC) or 9-bit (ECC) Bytes	blank = 8-bit Byte ECC = 9-bit Byte	
D	Core Org	Core organization	4i, 32s	
E	Memory Speed	Data transfer speed for RDRAM devices	800, 1066	MHz
F	t_{RAC}	Row Access Time (optional field)	-35, 40, -45 or blank	ns
G	Gerber Version	PCB Gerber file revision used on RIMM module (optional field)	Rev 1.00 = G100 or blank	-
H	SPD Version	SPD code version (optional field)	Rev 1.00 = S100 or blank	-
J	Vendor	Vendor specific part no., date code, mfg codes		
K	Vendor	Vendor specific barcode information (optional field)		
L	Vendor	Vendor logo area, country of origin		

Table Of Contents

Document: DL0114 Version: 0.1

Rambus Inc.
4440 El Camino Real
Los Altos, California USA
94022

Telephone: 650-947-5000
Fax: 650-947-5001
Internet: http://www.rambus.com