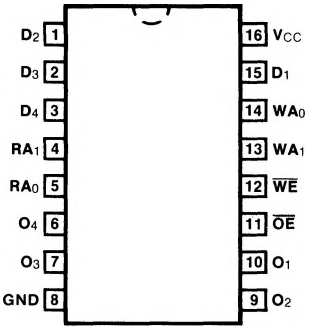
54LS/74LS670

4 X 4 REGISTER FILE

(With 3-State Outputs)

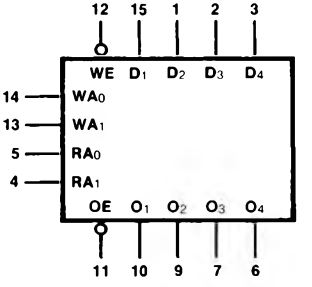
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '670 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 X 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

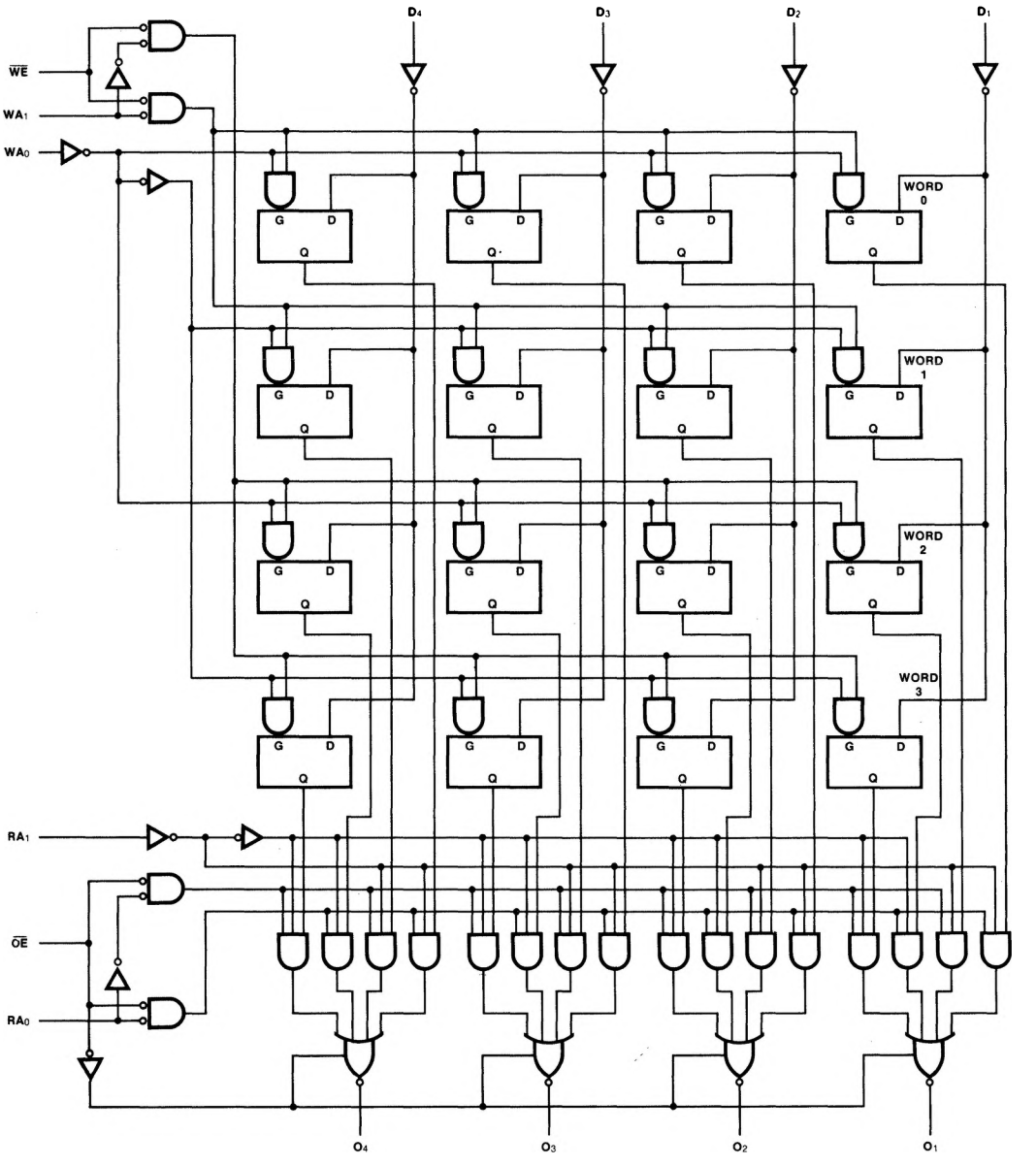
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10% TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS670PC		9B
Ceramic DIP (D)	A	74LS670DC	54LS670DM	6B
Flatpak (F)	A	74LS670FC	54LS670FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_1 - D_4$	Data Inputs	0.5/0.25
WA_0, WA_1	Write Address Inputs	0.5/0.25
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/0.5
RA_0, RA_1	Read Address Inputs	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.5/0.75
$O_1 - O_4$	Data Outputs	65/5.0 (25)/(2.5)

LOGIC DIAGRAM



WRITE FUNCTION TABLE

WRITE INPUTS			D INPUTS TO
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

READ FUNCTION TABLE

READ INPUTS			OUTPUTS FROM
$\overline{OE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

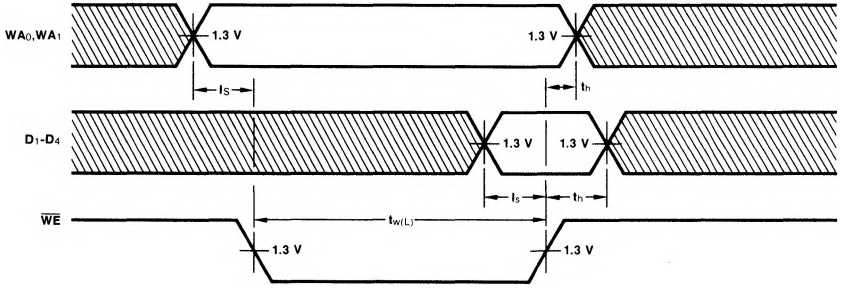


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		50	mA	V_{CC} = Max; WA_n, RA_n = Gnd; D_n, $\overline{WE}$ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay RA_0 or RA_1 to O_n		35 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to O_n		35 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		35 35	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		30 35	ns	Figs. 3-3, 3-11, 3,12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		40 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s	Setup Time HIGH or LOW D_n to Rising $\overline{WE}$	10		ns	Fig. a
t_h	Hold Time HIGH or LOW D_n to Rising $\overline{WE}$	10		ns	
t_s	Setup Time HIGH or LOW WA_n to Falling $\overline{WE}$	10		ns	
t_h	Hold Time HIGH or LOW WA_n to Rising $\overline{WE}$	5.0		ns	
t_w (L)	$\overline{WE}$ Pulse Width LOW	25		ns	Fig. a