National Semiconductor

54LS195A/DM74LS195A
4-Bit Parallel Access Shift Register

General Description

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

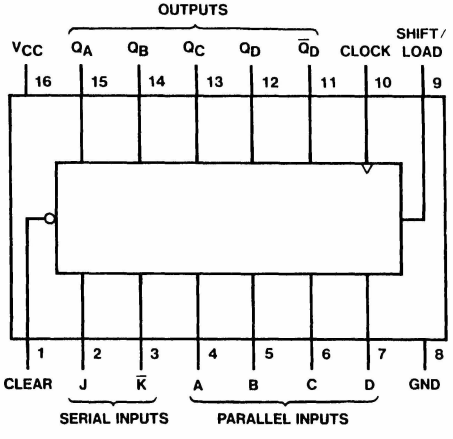
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 70 mW

Connection Diagram

Dual-In-Line Package



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Order Number 54LS195ADMQB, 54LS195AFMQB, 54LS195ALMQB, DM74LS195AM or DM74LS195AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS195A			DM74LS195A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		30		0	0		30	MHz
	Clock Frequency (Note 2)		30		0	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	16			16			ns
		Clear	14			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Shift/Load Release Time (Note 3)		10			10			ns
	Clear Release Time (Note 3)		25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74LS	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74LS		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74LS	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 6)			14	21	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS R_L = 2 kΩ C_L = 50 pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		21		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		24		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		26		38	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

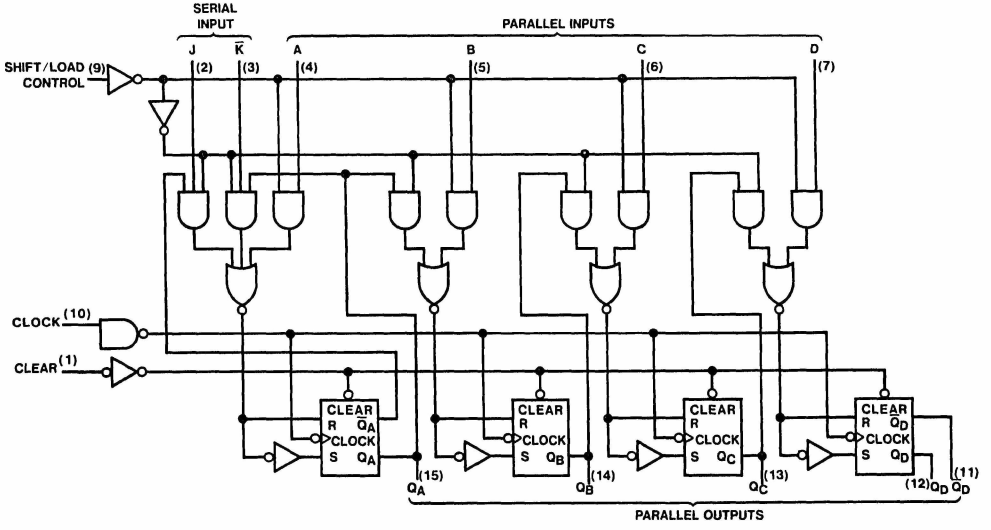
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

Logic Diagram



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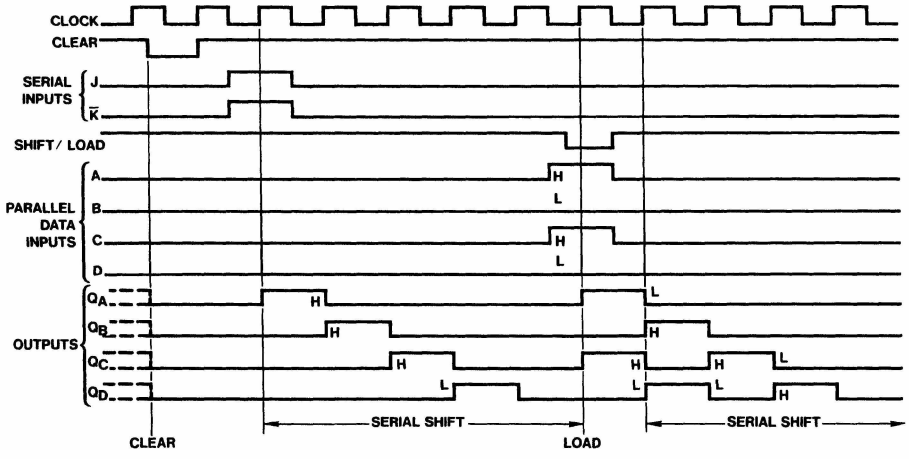
Timing Diagram

Typical Clear, Shift, and Load Sequences



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