# National Semiconductor

## 54173/DM54173/DM74173 TRI-STATE® Quad D Registers

## **General Description**

These four-bit registers contain D-type flip-flops with totempole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flipflops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

#### Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock elminates restrictions for operating in one of two modes: Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW
- Alternate Military/Aerospace device (54173) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.



### **Function Table**

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	Clock	Data E	Enable	Data	Output Q	
Clear		G1	G2	D		
Н	x	х	х	Х	L	
L	L	х	Х	х	Q <sub>0</sub>	
L	1	н	x	X	Q <sub>0</sub>	
L	1	х	н	X	Qo	
L	Î ↑	L	L	L	L	
L	1	L	L	н	н	

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

 $\mathbf{Q}_{\mathbf{Q}}=$  the level of  $\mathbf{Q}$  before the indicated steady state input conditions were established

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#### Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	-55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

### **Recommended Operating Conditions**

Symbol V <sub>CC</sub>	Parameter		DM54173			DM74173			Unito
			Min	Nom	Max	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High Level Input	Voltage	2			2			V
VIL	Low Level Input	Voltage			0.8			0.8	V
Юн	High Level Outpu	ut Current			-2			-5.2	mA
lol	Low Level Outpu	it Current			16			16	mA
fCLK	Clock Frequency	(Note 4)	0		25	0		25	MHz
tw	Pulse Width	Clock	20			20			ne
	(Note 4)	Clear	20			20			115
ts∪	Setup Time	Enable	17			17			ne
	(Note 4)	Data	10			10			115
tн	Hold Time	Enable	2			2			ne
1)	(Note 4)	Data	10			10			115
t <sub>REL</sub>	Clear Release Ti	me (Note 4)	10			10			ns
TA	Free Air Operatir	ng Temperature	-55		125	0		70	°C

#### Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
Vi	Input Clamp Voltage	$V_{CC} = Min, I_I = -12 mA$	4			-1.5	ν
V <sub>OH</sub>	High Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$		2.4			v
V <sub>OL</sub>	Low Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IH} = Min, V_{IL} = Max$				0.4	v
lı	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA
IIH	High Level Input Current	$V_{CC} = Max, V_I = 2.4V$				40	μΑ
I <sub>IL</sub>	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$				-1.6	mA
lozh	Off-State Output Current with High Level Output Voltage Applied	$V_{CC} = Max, V_O = 2.4V$ $V_{IH} = Min, V_{IL} = Max$				40	μΑ
I <sub>OZL</sub>	Off-State Output Current with Low Level Output Voltage Applied	$V_{CC} = Max, V_O = 0.4V$ $V_{IH} = Min, V_{IL} = Max$				-40	μΑ
los	Short Circuit	V <sub>CC</sub> = Max	DM54	-30		-70	mΑ
	Output Current	(Note 2)	DM74	-30		-70	mA
Icc	Supply Current	V <sub>CC</sub> = Max (Note 3)			50	72	mA

Note 1: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

Note 2: Not more than one output should be shorted at a time.

Note 3: I<sub>CC</sub> is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5V: N, G1, G2 and all DATA inputs grounded: and the CLOCK input and M input at 4.5V.

Note 4:  $T_A = 25^{\circ}C$  and  $V_{CC} = 5V$ .

Switchi	ng Characteristics at	$V_{CC} = 5V$ and $T_A = 2$	25°C (See Se	ection 1 for	Test Wavefo	rms and Ou	tput Load)
		From (Input) To (Output)					
Symbol	Parameter		C <sub>L</sub> = 5 pF		C <sub>L</sub> = 50 pF		Units
			Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency				25		MHz
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	Clock to Output				25	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	Clock to Output				28	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	Clear to Output				27	ns
t <sub>PZH</sub>	Output Enable Time to High Level Output	Output Control to Q			7	30	ns
t <sub>PZL</sub>	Output Enable Time to Low Level Output	Output Control to Q			7	30	ns
t <sub>PHZ</sub>	Output Disable Time from High Level Output	Output Control to Q	3	14			ns
t <sub>PLZ</sub>	Output Disable Time from Low Level Output	Output Control to Q	3	20			ns

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