DESCRIPTION

The 537 is a precision operational amplifier featuring very low input bias over the full temperature range, high gain, short circuit immunity, full input protection, simple compensation, excellent temperature stability, with offset voltage null capability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP
- LOW INPUT BIAS AND OFFSET

ABSOLUTE MAXIMUM RATINGS

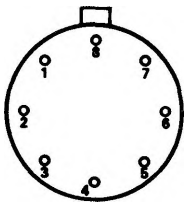
Supply Voltage	
SE537	±22V
NE537	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	±Vs
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE537	-55°C to +125°C
NE537	0°C to +70°C
Lead Temperature	300°C
Output Short Circuit Duration (Note 2)	Indefinite

NOTES:

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperature above +5°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATION

T PACKAGE
(Top View)

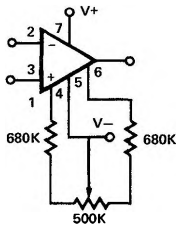


1. Freq. Comp / Offset Null
2. Inverting input
3. Noninverting input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

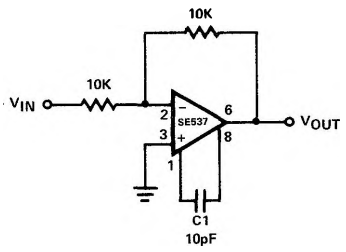
ORDER PART NOS. SE537T/NE537T

TEST CIRCUITS

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT

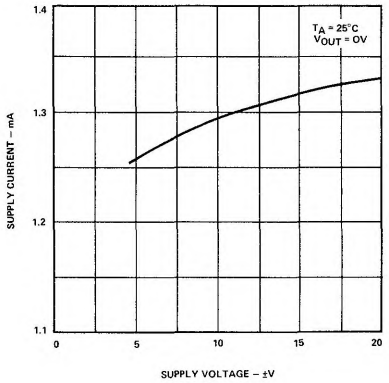


ELECTRICAL CHARACTERISTICS (V_S = ± 5V to ±20V unless otherwise specified.)

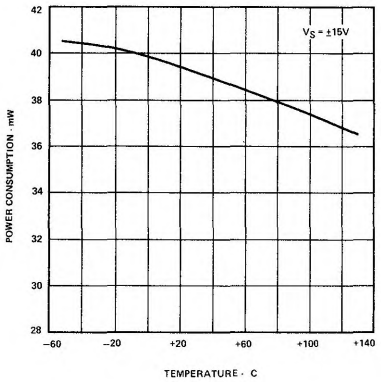
PARAMETER	CONDITIONS	NE537			SE537			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Input Offset Voltage	T_A = +25 °C		1.6	7.5		0.6	2.0	mV
Input Offset Voltage			2.0	10.0		1.2	3.0	mV
Input Offset Current	T_A = +25 °C		0.2	1.0		0.07	0.2	nA
Input Offset Current			0.25	1.5		0.12	0.3	nA
Input Bias Current	T_A = +25°C		1.5	7.0		0.8	2.0	nA
Input Bias Current			2.2	10.0		1.5	3.0	nA
Input Resistance		10	50		30	70		mΩ
Input Capacitance			0.5			0.5		pF
Offset Voltage Adjust Range			±15			±15		mV
Input Voltage Range	V_S = ±15V	±12	±14		±12	±14		V
Large Signal Voltage Gain	$R_L \geq$ 2k, V_{out} ±10V, V_S ±15V, T_A = 25°C	25k	400k		50k	500k		
Large Signal Voltage Gain	$R_L \geq$ 2k, V_{out} ±10V, V_S ±15V	16k	250k		25k	300k		
Output Resistance			75			75		Ω
Short Circuit Current	T_A = +25 °C		25			25		mA
Supply Voltage Rejection Ratio		80	100		80	100		dB
Common Mode Rejection Ratio	V_{in} = ±12V	80	100		86	100		dB
Supply Current	T_A = +25 °C		1.25	2.0		1.20	1.50	mA
Supply Current			1.30	3.0		1.30	2.0	mA
Unity Gain Frequency	V_S = ± 15V, C_C = 10pf		250			250		KHz
Slew Rate	V_O = ±5V, C_C = 10pF, R_L = 2kΩ		0.2			0.2		V/μsec
Output Voltage Swing	$R_L \geq$ 10k, V_S ±15V, C_L = 100pF	±13	±13.5		±13	±13.5		V
	$R \geq$ 2kΩ	±10	±12.6		±10	±12.6		V
Temperature Range		-0		+75	-55		+125	°C

TYPICAL PERFORMANCE CHARACTERISTICS

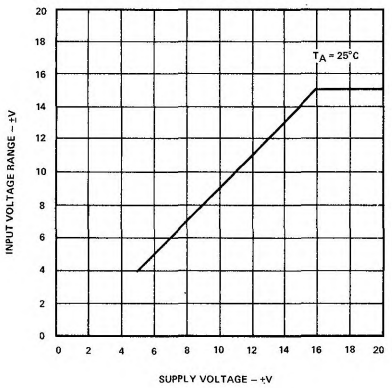
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

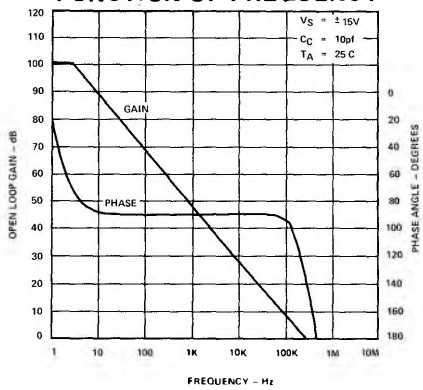


INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

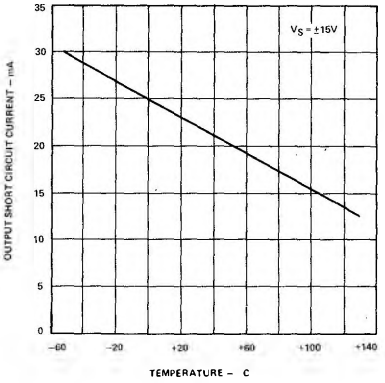


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

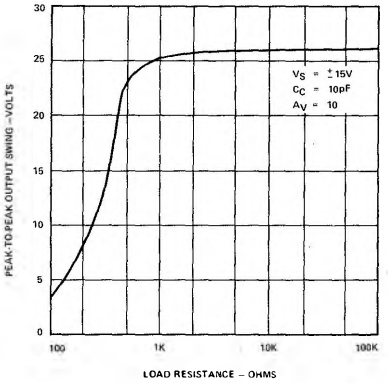
OPEN LOOP PHASE RESPONSES AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



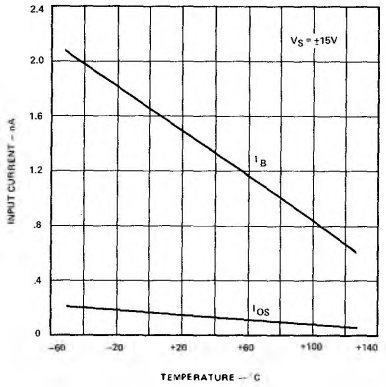
OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



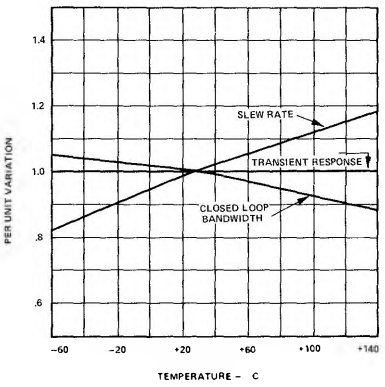
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



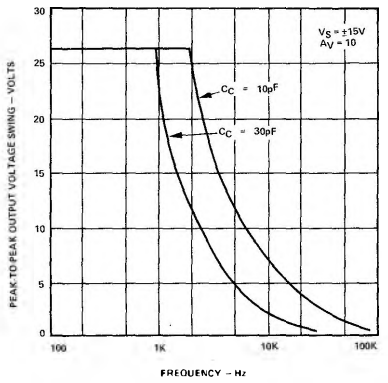
INPUT BIAS AND OFFSET CURRENTS AS FUNCTIONS OF AMBIENT TEMPERATURE



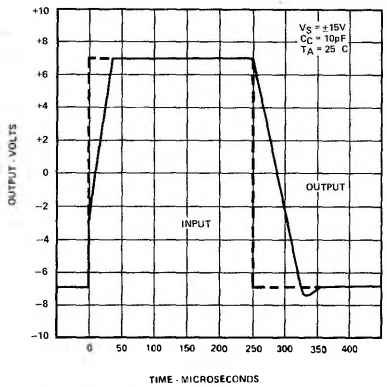
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



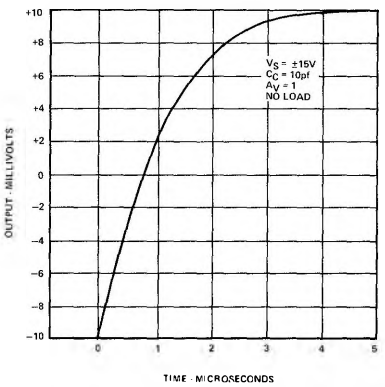
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



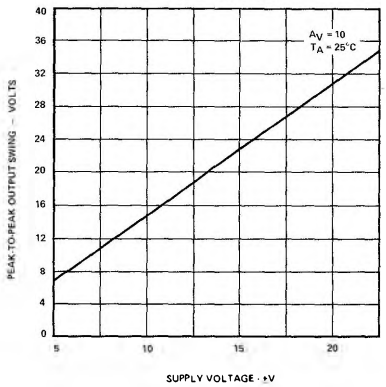
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE

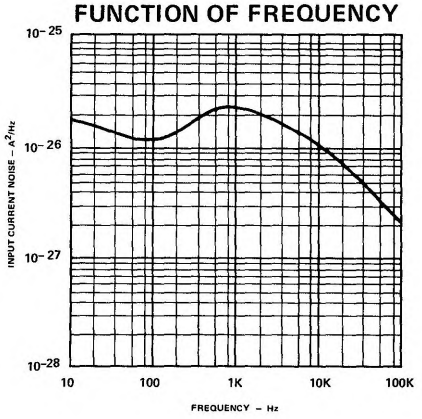


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

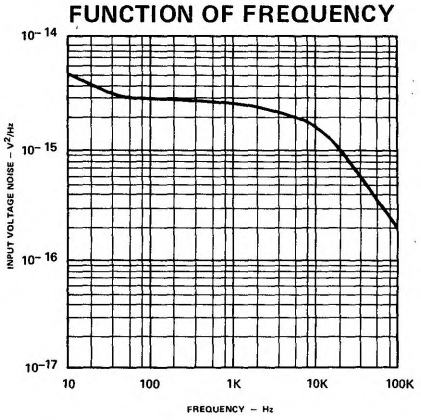


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

INPUT CURRENT NOISE AS A FUNCTION OF FREQUENCY



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



INPUT GUARD FOR LEAKAGE

Even with cleaned and coated boards, leakage currents can be comparable to the input bias current of the SE537. In addition the 537, as well as most other operational amplifiers, has its input pins adjacent to pins at the supply potential. In order to prevent leakage it is advisable to guard the input pins with a circuit board trace to ground.

PRINTED CIRCUIT LAYOUT FOR INPUT GUARDING

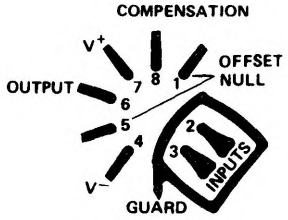


FIGURE 3a₀

INVERTING AMPLIFIER

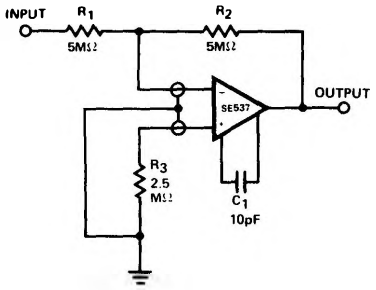


FIGURE 3b₀

NON-INVERTING AMPLIFIER

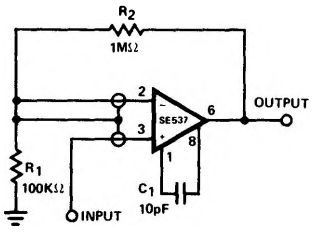
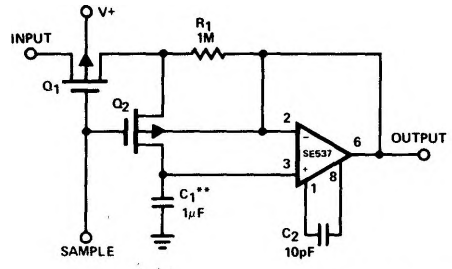


FIGURE 3c₀

TYPICAL APPLICATIONS

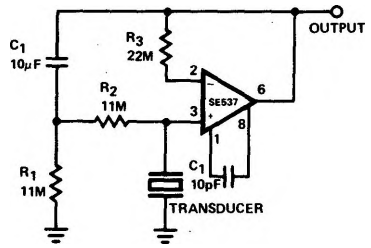
SAMPLE AND HOLD*



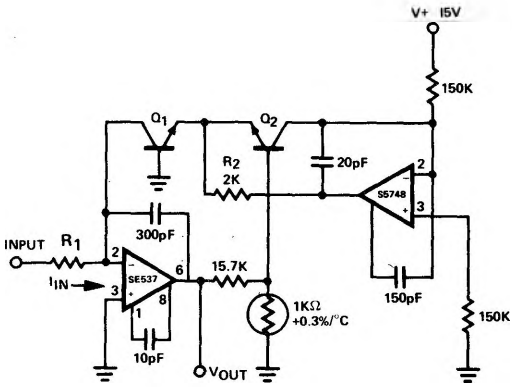
*WORST CASE DRIFT LESS THAN 2.5mV/sec

** TEFLON, POLYETHYLENE OR OR POLYCARBONATE DIELECTRIC CAPACITOR

AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS

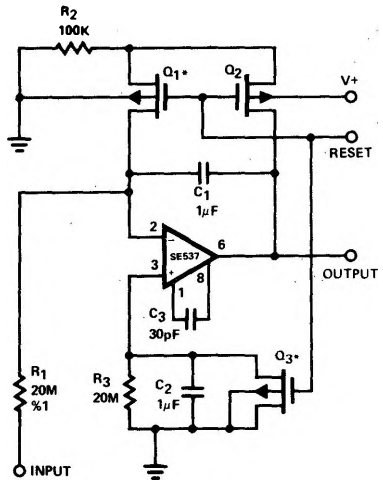


TEMPERATURE COMPENSATED LOGARITHMIC CONVERTER

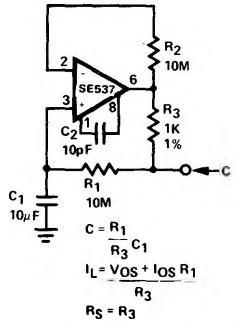


10nA< I_{IN} < 1mA
SENSITIVITY 1 V/ DECADE
"O" LEVEL 100μA

LOW DRIFT INTEGRATOR WITH RESET



CAPACITANCE MULTIPLIER

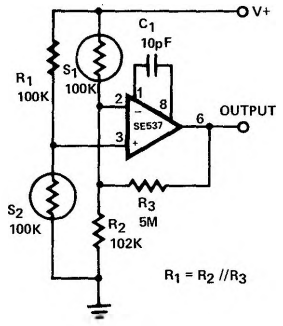


$C = \frac{R_1}{R_3} C_1$

$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$

$R_S = R_3$

AMPLIFIER FOR BRIDGE TRANSDUCERS



$R_1 = R_2 // R_3$