

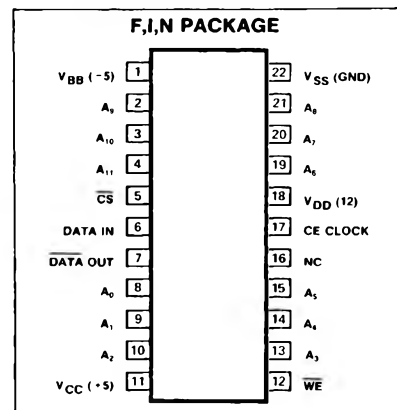
DESCRIPTION

The 2680 incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

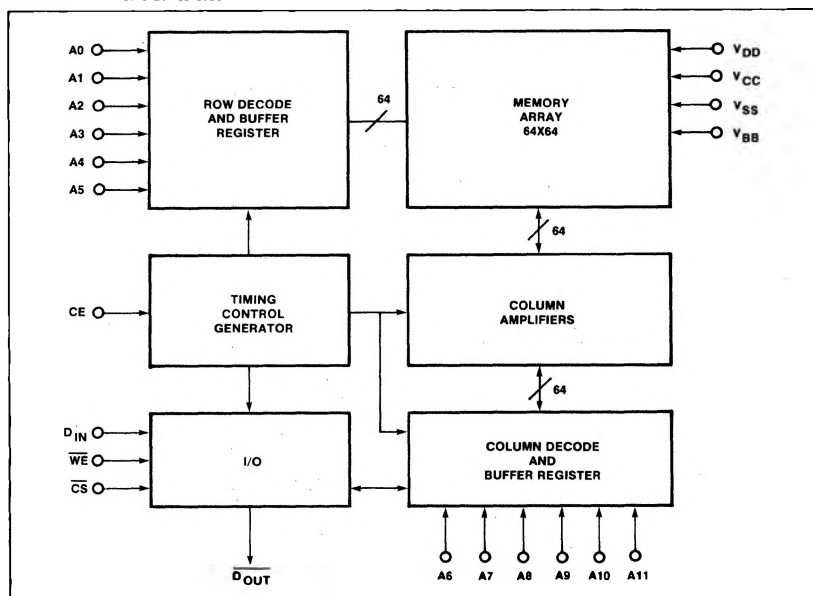
The 2680 must be refreshed every 2ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A_0 - A_5). The chip select input can be either high or low for refresh.

The 2680 has been designed with minimum production costs as a prime criterion. It is fabricated using n-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The 2680 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance and low cost memory device.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
T_A Temperature range	0 to 70	$^{\circ}\text{C}$
T_{STG} Operating under bias	-65 to 150	
P_D Storage	1.25	W
Power dissipation	20 to -0.3	V
All input or output voltages with respect to the most negative supply voltage, V_{BB}	20 to -0.3	V
Supply voltages V_{DD} , V_{CC} , and V_{SS} with respect to V_{BB}		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
Supply voltage				V
V _{CC}	4.75	5	5.25	
V _{DD}	11.4	12	12.6	
V _{SS}		0		
V _{BB}	-4.5	-5	-5.5	

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
Input voltage					V
V _{IL} Low		-1.0		0.6	
V _{IH} High		2.4		V _{CC} + 1	
V _{ILC} CE low		-1.0		1.0	
V _{IHC} CE high		V _{DD} - 1		V _{DD} + 1	
Output voltage					V
V _{OL} Low	I _{OL} = 2.0mA	0.0		0.45	
V _{OH} High	I _{OH} = -2.0mA	2.4		V _{CC}	
Input load current					μA
I _{LC} CE	V _{IN} = 0 min to V _{IHC} max		.01	2	
I _{LI} All inputs except CE	V _{IN} = 0 min to V _{IH} max, CE = V _{ILC} or V _{IHC}		.01	10	
I _{LO}	Output leakage current high impedance state		.01	10	μA
Supply current (V _{DD})					μA
I _{DD1} During CE off ³	CE = - 1V to 6V		50	200	
I _{DD2} During CE on	CE = V _{IHC} , $\overline{\text{CS}}$ = V _{IL}			60	mA
I _{DDAV1} Average V _{DD} current	Cycle time = 400ns, $\overline{\text{CS}}$ = V _{IL} , t _{CE} = 230ns, T _A = 25°C		35	54	mA
Supply current					μA
I _{CC1} V _{CC} ⁴	CE = V _{ILC} or $\overline{\text{CS}}$ = V _{IH}		.01	10	
I _{BB} V _{BB}			5	100	
Capacitance ⁵					pF
C _{AD} Address, CS	V _{IN} = V _{SS}		4	6	
C _{CE} CE	V _{IN} = V _{SS}		13	25	
C _{IN} Input and $\overline{\text{WE}}$	V _{IN} = V _{SS}		5	10	
C _{OUT} Output	V _{OUT} = OV		4	7	

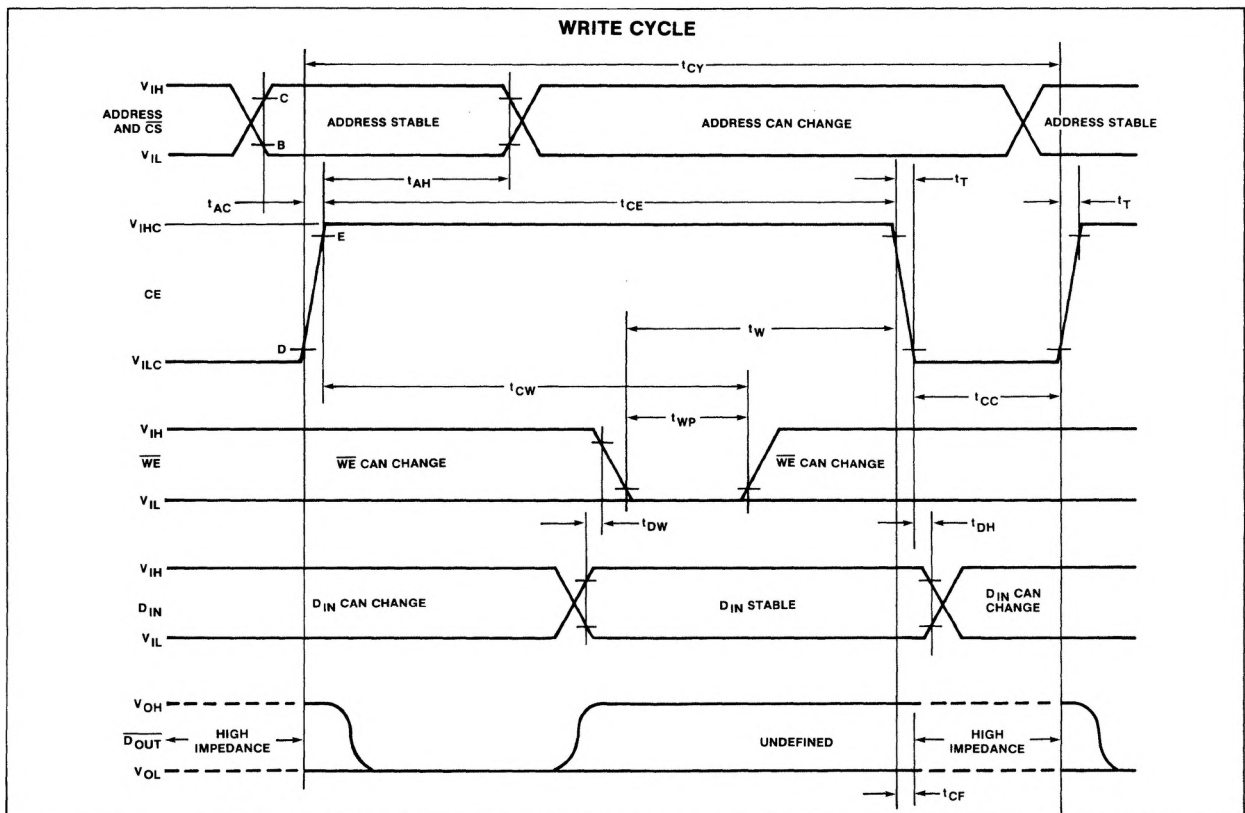
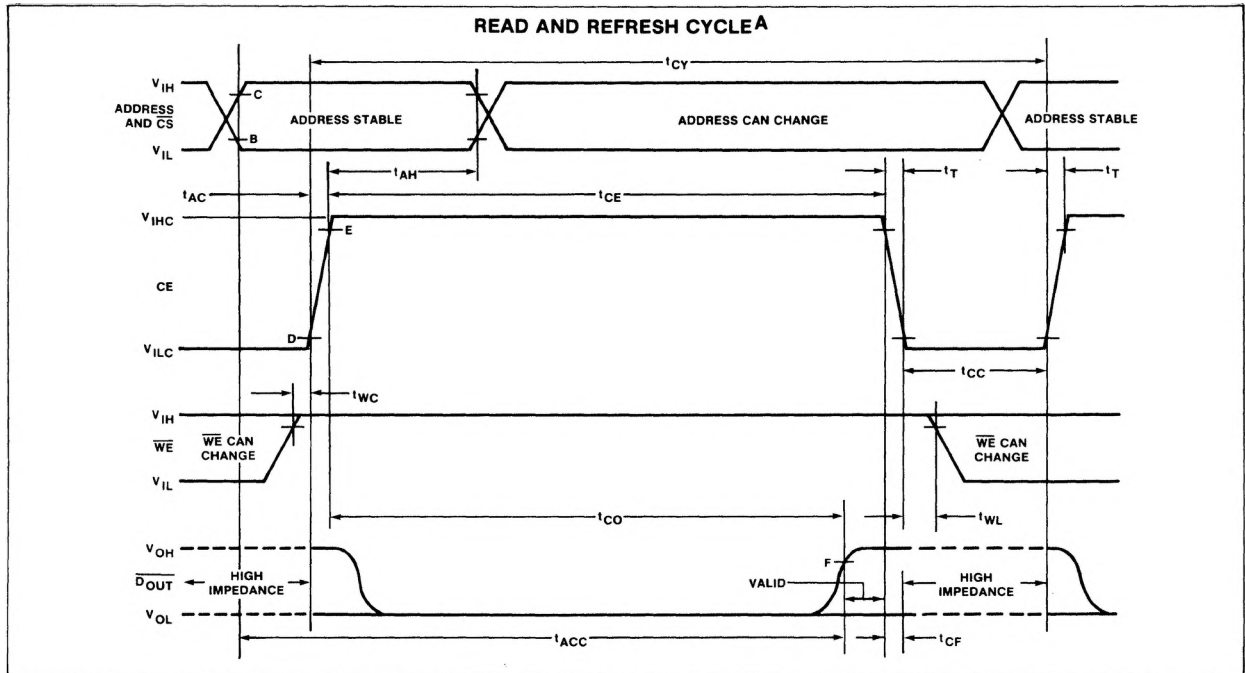
AC ELECTRICAL CHARACTERISTICS Over recommended supply voltage range, $T_A = 0^\circ\text{C}$ to 70°C , $t_r = 20\text{ns}$, $C_L = 50\text{pF}$,Load = 1 TTL gate, $t_{\text{ACC}} = t_{\text{AC}} + t_{\text{CO}} + 1t_r$

PARAMETER	TO	FROM	2680			2680-1			2680-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{REF} READ, WRITE, AND READ MODIFY/ WRITE CYCLE Time between refresh					2			2			1	ms
t_{AC} t_{AH} Setup and hold time Setup time Hold time	CE Address	Address CE	0 100			0 100			10 100			ns
t_{CC} t_r t_{CF} CE off time CE transition time CE high impedance state			130 10 0		40	130 10 0		40	380 10 0		40	ns ns ns
t_{CY} t_{CE} t_{CO} t_{ACC} t_{WL} t_{WC} READ CYCLE Cycle time CE on time CE output delay time Access time			400 230		4000 180 200	470 300		4000 250 270	800 380		4000 320 350	ns ns ns ns ns ns
t_{CY} t_{CE} t_w t_{CW} WRITE CYCLE Cycle time CE on time			400 230 150 150		4000	470 300 150 150		4000	800 380 200 150		4000	ns ns ns ns
t_{DW} t_{DH} Setup and hold time Setup time ^a Hold time	$\overline{\text{WE}}$ D_{IN}	D_{IN} CE	0 0			0 0			0 0			ns
t_{WP} Pulse width $\overline{\text{WE}}$			50			50			100			ns
t_{RWC} t_{CRW} t_w t_{WC} READ, MODIFY, WRITE CYCLE Cycle time CE width during cycle			520 350 150 0		4000	590 420 150 0		4000	960 540 200 0		4000	ns ns ns ns
t_{DW} t_{DH} Setup and hold time Setup time Hold time	$\overline{\text{WE}}$ D_{IN}	D_{IN} CE	0 0			0 0			0 0			ns
t_{WP} Pulse width $\overline{\text{WE}}$			50			50			100			ns
t_{CO} t_{ACC} Delay time Access time	Output	CE			180 200			250 270			320 350	ns ns

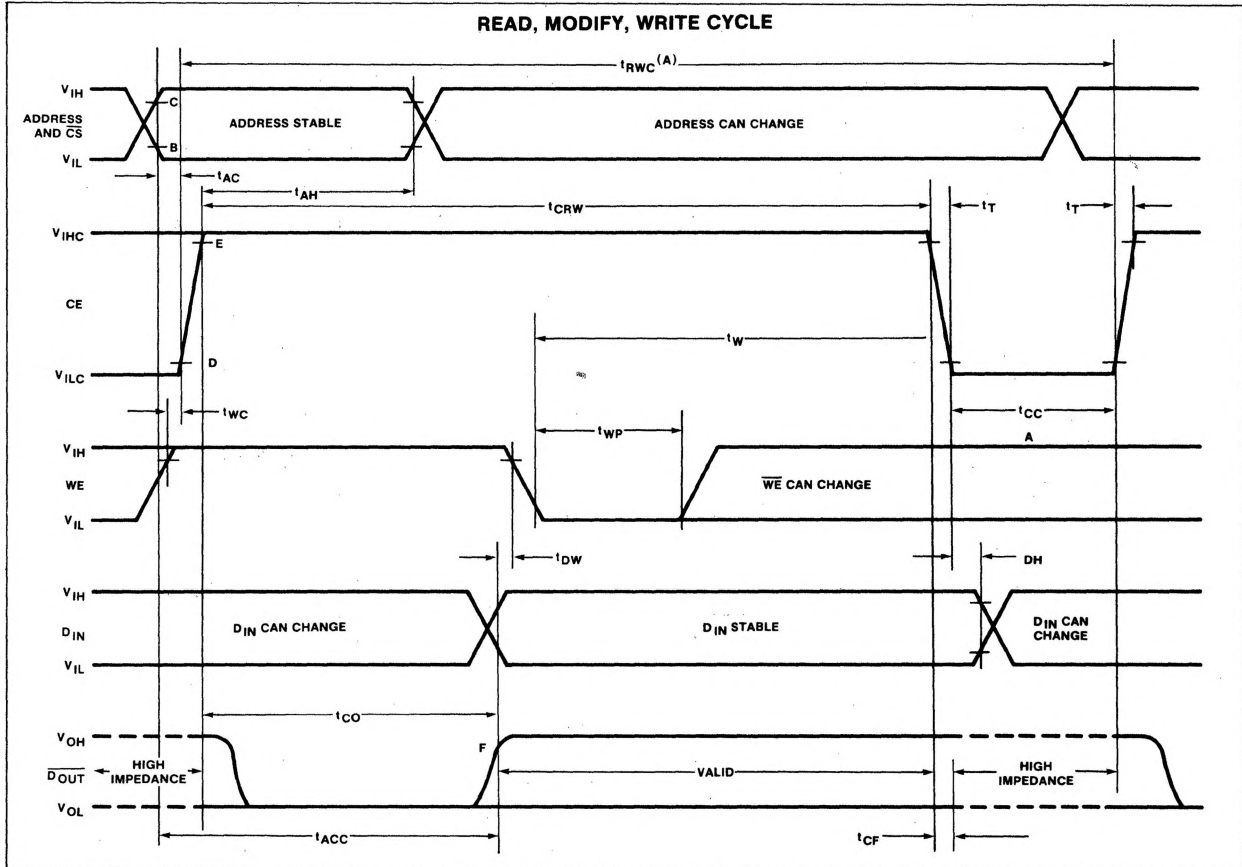
NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Typical values are for $T_A = 25^\circ\text{C}$ and typical power supply voltages.
- The I_{DD} and I_{CC} currents flow to V_{SS} . The I_{BA} current is the sum of all leakage currents.
- During CE on V_{CC} supply current is dependent on output loading V_{CC} is connected to output buffer only.
- Capacitance measured with Boonton Meter or effective capacitance calculated from the equation with the current equal to a constant 20mA.
- If $\overline{\text{WE}}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
- The only requirement for the sequence of applying voltage to the device is that V_{DD} , V_{CC} , and V_{SS} should never be .3V more negative than V_{BB} .

TIMING DIAGRAMS



TIMING DIAGRAMS (Cont'd)



NOTES

- A. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
- B. V_{IL} max is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN} .
- C. V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN} .
- D. $V_{SS} + 2.0V$ is the reference level for measuring timing of $\overline{CE}$.
- E. $V_{DD} - 2V$ is the reference level for measuring timing of $\overline{CE}$.
- F. $V_{SS} + 2.4V$ is the reference level for measuring the timing of D_{OUT} .