DESCRIPTION

The Signetics 2656 System Memory Interface (SMI) is a mask programmable circuit with on-chip memory, I/O, and timing (clock) functions. It is useable either in 2-chip or multi-chip microcomputer systems. Used with the 2650 microprocessor, it provides a 2-chip microcomputer. This 2-chip microcomputer offers the user 2KX8 bits of ROM, 128X8 bits of RAM, and an 8-bit input-output port.

Used as a system interface in a multi-chip microcomputer, with larger memory and/or additional peripheral requirements, the programmable versatility of the SMI provides decoded chip enable outputs. These outputs connect directly to other memory or I/O functional blocks with few and often no requirement for additional interfacing chips. This reduces both chip count and cost in complex microcomputer systems.

The 2656 is processed using Signetics n-channel silicon gate technology. Only a single power supply of +5 volts is needed for operation.

FEATURES

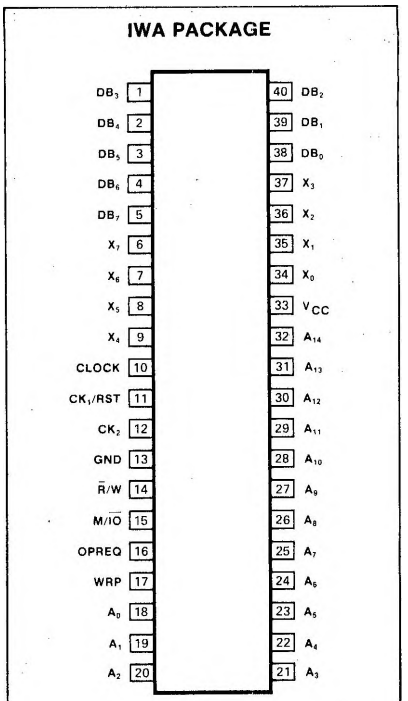
- **2KX8 mask programmable ROM**
- **128X8 static RAM**
- **8 multi-purpose pins for either chip enables or I/O bits**
- **8-bit latch for either I/O or MPU storage**
- **Internal clock generator with crystal, RC, or external timing source**
- **System power-on reset**
- **40-pin dual-in-line package**
- **Single +5 volt supply**

APPLICATIONS

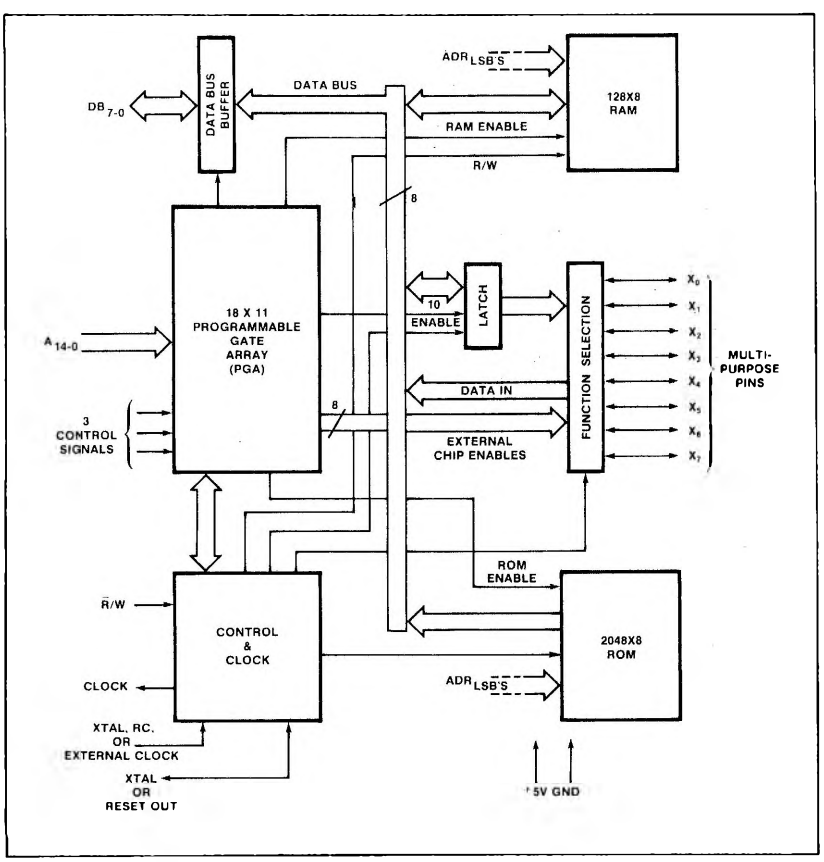
- **2-chip microcomputer**
- **System control for multi-chip microcomputers—eliminates or reduces TTL suppport circuitry for memory and I/O device selection.**
- **From small (2K-2 chip) to 32K microprocessor-based systems**

PIN CONFIGURATION

IWA PACKAGE



BLOCK DIAGRAM



FUNCTIONAL BLOCK DESCRIPTIONS

Data Bus Buffer

A tri-state bidirectional 8-bit bus transceiver for data transfer between the SMI and MPU.

Programmable Gate Array (PGA)

Provides select signal outputs for the internal ROM, RAM, Latch, and up to 8 multi-purpose I/O pins that are mask programmed as Chip Enables. A PGA output is active when the input variables match any one of 11 corresponding mask programmed product terms. The 18 input variables are normally address and control bus signals from the MPU and may be programmed as "1", "0", and "don't care." Each product term is a specified combination of the input variables.

Control and Clock

Generates the Clock output signal to the MPU and control signals for the ROM, RAM, and Latch. A mask programmable frequency divider provides input frequency division by 1, 2, 3, or 4. The timing source is mask programmable and may be a crystal, RC, or external oscillator. If either of the latter two are designated as a timing source, the second timing pin becomes a Reset output to the MPU.

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB_0-DB_7	38-40 1-5	I/O	**8-bit Bidirectional Data Bus:** All data transfers between the MPU and ROM, RAM, Latch, and X pins are made using this bus.
A_0-A_{14}	18-32	I	**MPU Address Bus:** Address bus inputs occupy contiguous bit positions with A_0 as the least significant address bit.
OPREQ	16	I	**Control Signal:** A signal that specifies the valid state of address and control bus.
M/$\overline{IO}$, WRP	15, 17	I	**Optional Signals:** Possibilities include Memory or I/O (M/$\overline{IO}$), Write Pulse (WRP), external control signals, or additional high order address bits.
$\overline{R}$/W	14	I	**Read/Write Control:** A control signal from the MPU that indicates whether the requested operation is to be a Read or Write (0 or 1 respectively). This signal must not change while OPREQ is true.
CLOCK	10	O	**Clock Output to the MPU:** The frequency is determined by the timing element and the mask programmable divisor (divided by 1, 2, 3, 4).
CK_1/RST, CK_2	11,12	I/O, I	**Connections for the Timing Element:** Only CK_2 is necessary for an RC or external timing source. The CK_1/RST pin then becomes a power-on Reset output. Two pins are necessary for direct connection of a crystal.
V_{CC}	33	I	**+5V:** Power supply.
GND	13	I	**Ground:** 0V reference ground.
X_0-X_7	34-37 9-6	I/O	**Multi-purpose I/O Pins:** These pins can be mask programmed as external memory or I/O chip enables, or bidirectional I/O port data bits, or any combination of the two.

ROM

2,048 bytes of mask-programmable Read Only Memory for storage of instructions and constants. The ROM base address is PGA mask programmable over the entire MPU address range. The ROM can be disabled by a mask option.

RAM

128 bytes of Read/Write Memory for MPU data storage and retrieval. The RAM base address is PGA mask programmable over the entire MPU address range. RAM dominates over ROM if address overlap is intentionally mask programmed. The RAM can be disabled by a mask option.

Function Select

A 1X8 Function Select array of mask-programmable contacts determine the function of each of the multi-purpose I/O pins (X_0-X_7). Two modes exist:

1. CE - The X pin is an active low Chip Enable ($\overline{CE}$) for either external memory or an I/O port. PGA inputs receive the external address and MPU control signals required to generate the $\overline{CE}$ output.
2. P - The X pin is a bidirectional I/O port data bit. A portion of the PGA provides the control signal to select the port.

Latch

Holds output data for the multi-purpose I/O pins mask programmed as a mode P. The latch continues to function as a read/write element even if all multi-purpose I/O pins are programmed as chip enables. Thus, any X pin that is programmed as an external chip enable can have corresponding latch bits available for temporary data storage or software flags. To read an input pin, the corresponding latch bit must first be written to a "one" by the MPU program. This is done to disable all active outputs, changing them to passive pullup outputs. This permits inputs to be sensed on the same pin. Subsequent reads of the same pin do not have to be preceeded by a write if the state of the latch pin remains a "one."

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	All voltages with respect to *ground*[3]	-0.5 to +6.0	V

NOTES

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operations section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 55°C/W junction to ambient (IWA ceramic package.)
3. This product includes circuitry specifically designed for this protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%[1,2,3,4,10]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-.5		0.8	
V_{IH}	High		2.2			
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.45	
V_{OH}	High	I_{OH} = -100μA[6]	2.4			
V_{OHP}	I/O port output high voltage	I_{OHP} = -50μA[7]	2.4			V
I_{IL}	Input load current	V_{IN} = 0 to 5.5V			10	μA
I_{LD}	Data bus leakage current	V_{OUT} = 4.0V			10	μA
I_{CC}	Power supply current				150	mA
	Capacitance	T_A = 25°C, V_{CC} = 0V				
C_{IN}	Input	f_c = 1MHz		4	10	pF
C_{OUT}	Output	Unmeasured pins		4	10	pF
$C_{I/O}$	I/O	tied to ground		6	10	pF

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%,[1,2,3,4,9,10]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_S	Address and control setup time		0			ns
t_H	Address and control hold time		0			ns
t_{PD1}	Propagation delay time - high to low[5]	C_L = 100pF	50		230	ns
t_{PD2}	Propagation delay time - low to high[5]	C_L = 100pF	50		230	ns
t_{WRP}	Write pulse width		200			ns
t_{DD}	Data bus delay time for read	C_L = 100pF	200		580	ns
t_{DF}	Data bus floating time for read	C_L = 100pF			580	ns
t_{DBS}	Data bus setup time for write		200			ns
t_{DBH}	Data bus hold time for write		200			ns
t_{OD}	Output delay time	C_L = 100pF	100		400	ns
f_C	Crystal or external clock frequency				4.0	MHz
t_C	External clock high or low state		110			ns
t_{RST}	Reset output pulse width[8]		30		300	μs
t_{AWS}	Address to write pulse setup time		50			ns

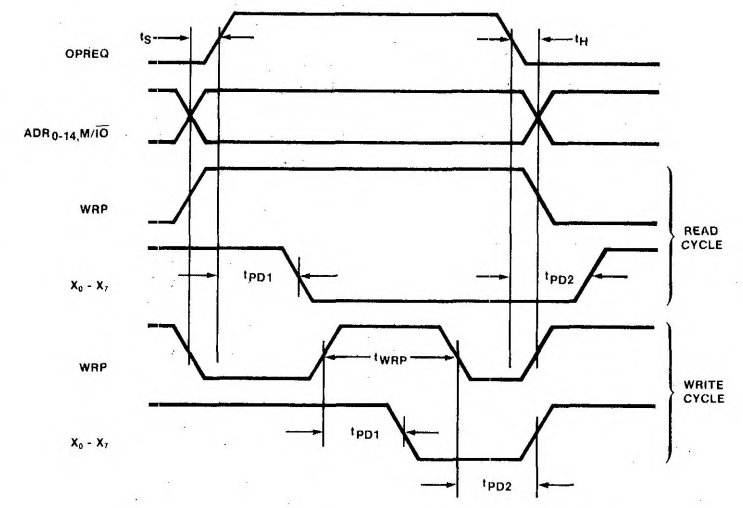
NOTES

1. Parameters are valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, V_{IL} levels as appropriate.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. AC characteristics assume the following input signals from a Signetics 2650 microprocessor:

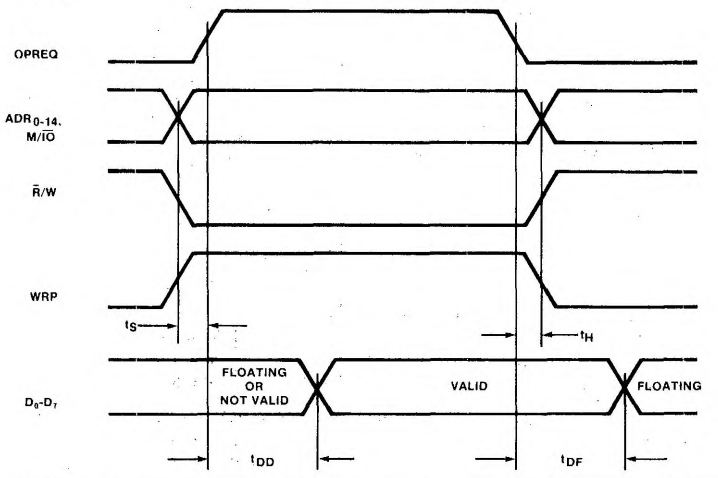
   Pins 18-32 = ADR_0-ADR_{14} Pin 15 = M/$\overline{IO}$
   Pin 16 = OPREQ Pin 17 = WRP
5. For X_0-X_7, time reference is OPREQ or time input changes, whichever is later.
6. Data Bus, Chip Enable, CK_1/RST or Clock outputs.
7. Port outputs only.
8. V_{CC} rise time must be less than 100 microseconds.
9. The delay times (Minima and Maxima) tend to track each other for any single device.
10. This is not a final specification. Parametric limits are subject to change.

TIMING DIAGRAMS

X_0-X_7 PINS USED AS CHIP ENABLES

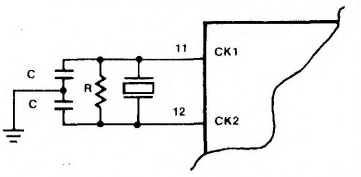


READ CYCLE (FOR ROM, RAM, LATCH, OR X_0-X_7 PINS USED AS INPUTS)



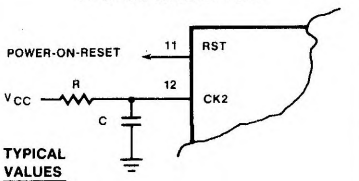
CLOCK CONFIGURATIONS

CRYSTAL CONNECTION



C = 15pF typical R = 1MΩ typical

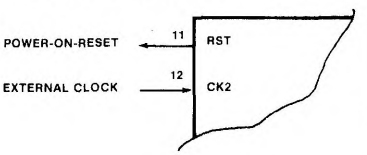
R-C CONNECTION



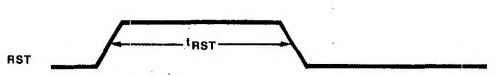
TYPICAL VALUES

f	R	C
2MHz	20K	20pF

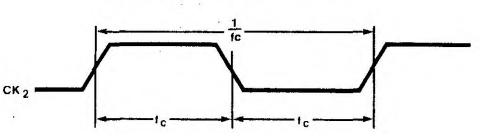
EXTERNAL CLOCK CONNECTION



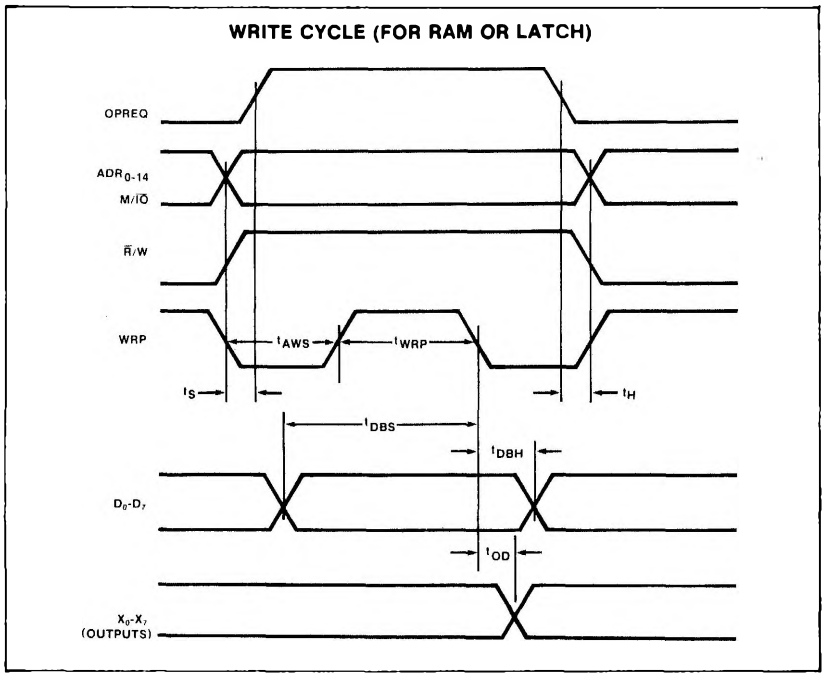
RESET OUTPUT



EXTERNAL CLOCK INPUT



TIMING DIAGRAMS (Cont'd)



CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

A computer-aided technique utilizing punched computer cards is employed to specify a custom version of the 2656. This technique requires that the customer supply Signetics with a deck of standard 80-column computer cards describing the data to be stored in the ROM array, the Programmable Gate Array (PGA), and the Function Select Array.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer-Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

The contents of each card in the deck are:

Customer Identification Cards are always labeled with a "C" in column 1. For customer identification any number of cards is permitted. A 4-card example is shown below. The following data should be included:

COLUMN	DATA
1	C
2	Blank
3-66	Company name (Card #1) Street address (Card #2) City, State, Zip (Card #3) Contact person name (Card #4)
67	Blank
68-70	SMI
71	Blank
72-75	2656
76-78	Blank
79-80	2-digit decimal number indicating the truth table number. Must be the same on all cards in the deck.

(Explanatory Note: The next card for this example is card No. 5)

CARD #5—SMI FUNCTIONAL PARAMETERS

COLUMN	DATA
1-9	Blank

The next eight columns specify whether multi-purpose pins (X_0-X_7) are to be chip enables or I/O port data bits. Each column must contain either the character "E" for chip enable or the character "P" for I/O port. Card column 10 specifies X_0, card column 17 specifies X_7.

COLUMN	DATA
10	E or P for X_0
11	E or P for X_1
12	E or P for X_2
13	E or P for X_3
14	E or P for X_4
15	E or P for X_5
16	E or P for X_6
17	E or P for X_7
18-19	Blank

Select one of the next three columns to specify the type of clock source; crystal, external or R/C network. An "X" designates the selected clock source. The other two columns must be blank.

COLUMN	DATA
20	X or blank (Crystal)
21	X or blank (R/C Network)
22	X or blank (External)
23-29	Blank

Select one of the next four columns to specify the clock source divider value to divide by 1, 2, 3 or 4. An "X" designates the selected divisor. The other three columns must be blank.

COLUMN	DATA
30	X or blank (÷ 1)
31	X or blank (÷ 2)
32	X or blank (÷ 3)
33	X or blank (÷ 4)
34-39	Blank

Access to ROM, RAM or I/O Port bits may be disabled. The next three columns are used to disable ROM, RAM or I/O Port. Specify an "X" (disable) or blank (do not disable).

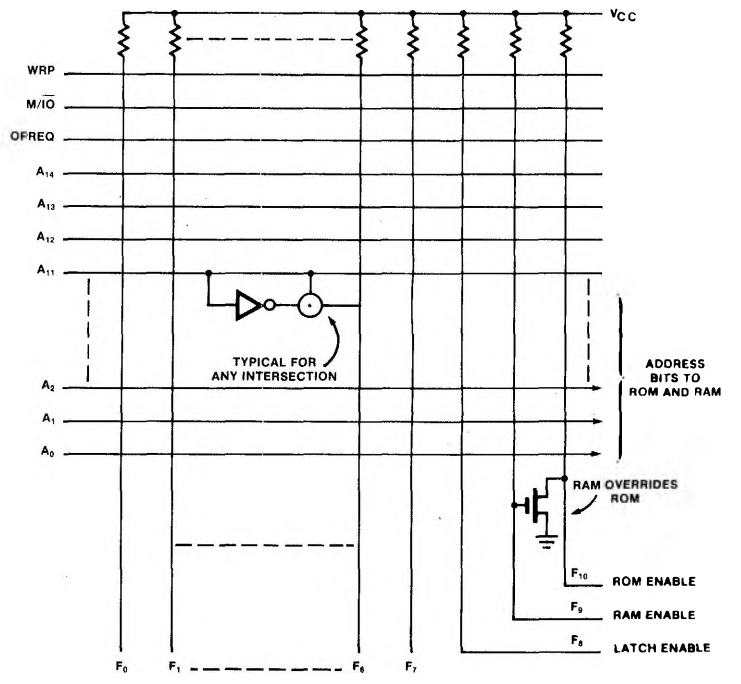
COLUMN	DATA
40	X or blank (ROM)
41	X or blank (RAM)
42	X or blank (PORT)
43-78	Blank
79-80	Two-digit decimal number indicating the truth table number.

CARD #6—PGA SPECIFICATION

The PGA is an 18 X 11 input-output structure. The first eight outputs are available as chip enables (if selected by the appropriate function—select parameters on card #5). The last three outputs are internally connected to enable the SMI internal I/O Port, RAM and ROM. (See Figure 1.) Ascending order of card columns correspond to ascending PGA outputs. Thus, columns 5 through 15 correspond, respectively, to PGA chip enable outputs 0 through 7, the latch enable, the RAM enable and the ROM enable. Valid characters are 1, 0 or X. "1" indicates active high, "0" indicates active low, and "X" indicates don't care.

COLUMN	DATA
1	A
2	0
3-4	Blank
5-15	1, 0 or X (A_0 for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_1 for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_2 for F_0 to F_{10})
40	Blank
41-51	1, 0 or X (A_3 for F_0 to F_{10})
52	Blank
53-63	1, 0 or X (A_4 for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (A_5 for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

PROGRAMMABLE GATE ARRAY (PGA)



NOTE

Each intersection can be programmed as active low (0), active high (1), or "don't care"(X).

Figure 1

CARD #7— PGA SPECIFICATION (Cont'd)

COLUMN	DATA
1	A
2	6
3-4	Blank
5-15	1, 0 or X (A_6 for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_7 for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_8 for F_0 to F_{10})
40	Blank
41-51	1, 0 or X (A_9 for F_0 to F_{10})
52	Blank
53-63	1, 0 or X (A_{10} for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (A_{11} for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

CARD #8— PGA SPECIFICATION (Cont'd)

COLUMN	DATA
1	A
2-3	12
4	Blank
5-15	1, 0 or X (A_{12} for F_0 to F_{10})
16	Blank
17-27	1, 0 or X (A_{13} for F_0 to F_{10})
28	Blank
29-39	1, 0 or X (A_{14} for F_0 to F_{10})
40	Blank
41-51	1, 0 or X ($M/\overline{IO}$ for F_0 to F_{10})
52	Blank
53-63	1,0 or X (OPREQ for F_0 to F_{10})
64	Blank
65-75	1, 0 or X (WRP for F_0 to F_{10})
76-78	Blank
79-80	2-digit decimal number indicating the truth table number.

BINARY ROM CODE FORMAT

CARD #9 THROUGH CARD #264

These remaining cards specify the 2048 8-bit locations of the SMI ROM. The first data field of card #9 is ROM location 0, the last data field of card #264 is ROM location 2047. For each field, the leftmost character is the MSB, the rightmost character is the LSB. Valid characters are 1 or 0. Alternately, P or N characters may be used. A "1" or "P" represents a logic high at the SMI data bus connection. A "0" or "N" represent a logic low. Each of these cards is configured as follows:

COLUMN	DATA
1-5	Right justified decimal address of first data field of the card (columns 7-14).
6	Blank
7-14	1 or 0; or, P or N

COLUMN	DATA
15	Blank
16-23	1 or 0; or, P or N
24	Blank
25-32	1 or 0; or, P or N
33	Blank
34-41	1 or 0; or, P or N
42	Blank
43-50	1 or 0; or, P or N
51	Blank
52-59	1 or 0; or, P or N
60	Blank
61-68	1 or 0; or, P or N
69	Blank
70-77	1 or 0; or, P or N
78	Blank
79-80	2-digit decimal number indicating the truth table number.

HEXADECIMAL ROM CODE FORMAT

CARD #9 THROUGH CARD #72

The customer may also submit ROM code in hexadecimal format. 32 locations (bytes) are specified on each card. Columns 7 and 8 of card #9 contain the data for ROM location 0 while columns 69 and 70 of card #72 contain the data for ROM location H'7EF'. In each data pair, the left character is the hexadecimal equivalent of bits D_7 to D_4; the right character is the hexadecimal equivalent of bits D_3 to D_0. Table 1 shows the conversion from binary to hexidecimal.

Each of these cards is configured as follows:

COLUMN	DATA
1-4	Right justified hexadecimal address of first data pair of the card (columns 7-8). For example, card #9 will contain '0000,' card #10 will contain '0020' and so forth until card #72, which contains '07E0.'
5-6	Blank
7-8	First data pair
9-10	Next data pair
11-12	Next data pair
11-12	Next data pair
11-12	Next data pair
11-12	Next data pair
67-68	Next to last data pair
69-70	Last data pair of card
71-78	Blank
79-80	2-digit decimal number indicating the truth table number.

BINARY COMBINATION D_7-D_4 OR D_3-D_0				HEXA-DECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

Table 1 BINARY TO HEXADECIMAL CONVERSION

APPLICATION EXAMPLES

A TWO CHIP MICROCOMPUTER

The minimum system depicted in Figure 2 is composed of the 2650 MPU, a 2656 SMI, and a resistor/capacitor network for a timing input. The SMI provides MPU CLOCK and RESET signals and eight I/O Port bits (X_0-X_7).

Note that because all eight I/O bits share the same device address, the MPU program must "housekeep" unwanted bits when reading or writing to any of them. If a one-bit write operation is desired, the MPU must preserve the state of all other output pins. This can be done by reading the latch, changing the state of the selected bit, and outputing the result.

Any latch bit used for input must first be written to a Logic "1" before a read operation. After reading the data, the bits not desired must be masked out by the program.

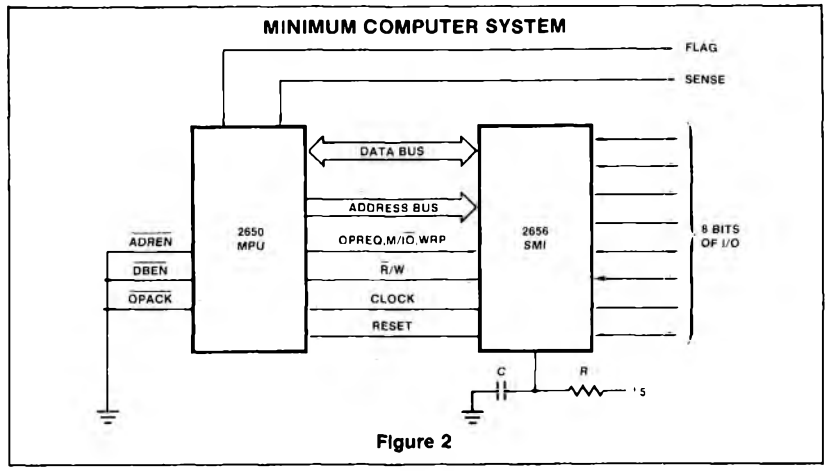


Figure 2

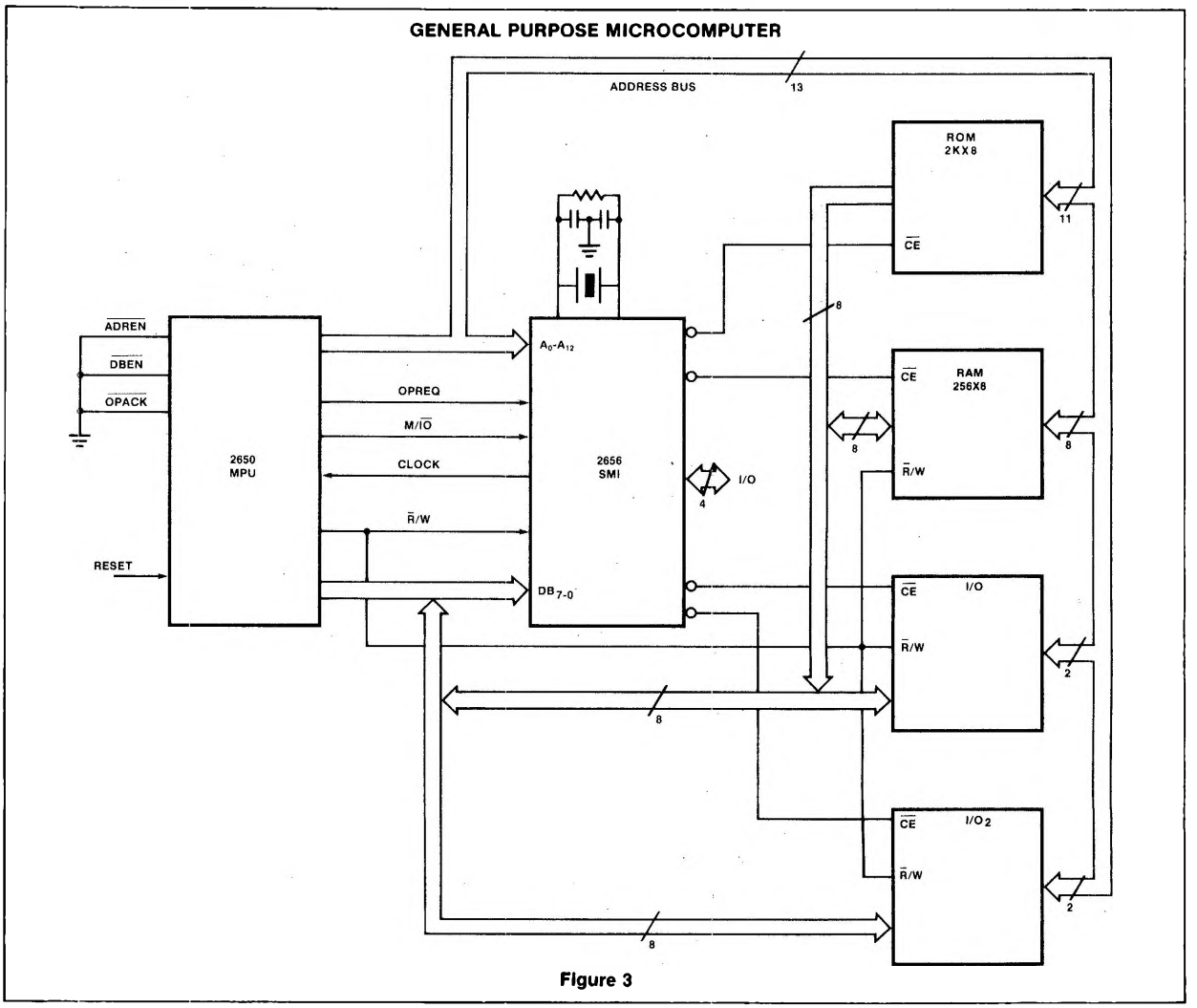


Figure 3

A GENERAL PURPOSE MICROCOMPUTER

A general purpose microcomputer is illustrated in Figure 3. The SMI provides ROM RAM and the MPU clock from a crystal source. It also provides chip enables for external ROM, RAM and LSI peripheral controllers 1 and 2 as well as four bidirectional data bits.

The state of M/$\overline{IO}$ in the Address Map (Table 6) indicates that I/O_1 and I/O_2 are memory mapped while the SMI port is referenced using any I/O instruction (extended or non-extended) on the 2650. See the SMI Program Table (Table 7).

The 2650 addresses the SMI port to input or output data on X_4-X_7. SMI latch bits 0-3 are available for MPU temporary storage since the corresponding X pins are used for external chip enables.

Note that the 13 MPU address bits are assigned to the first 13 PGA inputs (A_0-A_{12}) and that only two MPU control signals (OPREQ, M/$\overline{IO}$) are input to the PGA (WRP is not required).

The SMI uses the $\overline{R}$/W signal from the 2650 to read or write from the internal RAM and port. External devices are enabled when their address (A_0-A_{12}, M/$\overline{IO}$) have been decoded by the SMI and OPREQ is valid.

	PIN	# BYTES	ADDRESS	M/$\overline{IO}$
Internal ROM	—	2K	0000-07FF	1
External ROM	X_0	2K	0800-0FFF	1
*Spare ROM	—	1K	1000-13FF	1
External RAM	X_1	256	1400-14FF	1
Internal RAM	—	128	1500-157F	1
*Spare RAM	—	512	1600-17FF	1
I/O_1	X_2	4	1800-1803	1
I/O_2	X_3	4	1804-1807	1
SMI Port	—	—	ANY	0

*Space left for possible system expansion.

Table 6
ADDRESS MAP FOR GENERAL PURPOSE MICROCOMPUTER

	PRODUCT TERM																		
NO.	WRP	A14	A13	M/IO	OPREQ	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	FS*
0	X	X	X	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	E X_0
1	X	X	X	1	1	1	0	1	0	0	X	X	X	X	X	X	X	X	E X_1
2	X	X	X	1	1	1	1	0	0	0	0	0	0	0	0	0	X	X	E X_2
3	X	X	X	1	1	1	1	0	0	0	0	0	0	0	0	1	X	X	E X_3
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_4
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_5
6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_6
7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_7
8	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	PORT
9	X	X	X	1	1	1	0	1	0	1	0	X	X	X	X	X	X	X	RAM
10	X	X	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	ROM

DISABLE			PGA	XTL	R/C	EXT	1	2	3	4
			TIMING SOURCE	√				√		
ROM	RAM	PORT						CK Divide by		

*P = Port E = Enable

Table 7 SMI PROGRAM TABLE FOR GENERAL PURPOSE MICROCOMPUTER

HIGH PERFORMANCE MICROCOMPUTER SYSTEM

The six-chip high performance system of Figure 4 contains a 2655 Programmable Peripheral Interface and a 2651 Programmable Communication Interface. Two SMIs are used in the system. The first SMI provides CLOCK and RESET signals to the 2650, initial increments of ROM and RAM, and eight bits of bidirectional I/O to the user's external interface. The second SMI provides a crystal controlled clock for the PCI, additional amounts of ROM and RAM, read (RDS) and write (WRS) strobes for the first SMI's eight-bit port, chip enables for PPI and PCI, and four bits of bidirectional I/O data.

The PPI and PCI addresses are decoded by SMI #2 to generate the chip selects on X_7 and X_6. The two least significant MPU address bits specify one of three PPI eight bit I/O ports or one of four PCI internal registers. Three PCI interrupt conditions are WIRE-ORed (active low) to the 2650 interrupt request input (INTREQ). The interrupt acknowledge (INTACK) is inverted and used to enable the interrupt vector onto the data bus through the 74LS240 tri-state buffer.

	PRODUCT TERM																		
NO.	M/IO	A_{14}	A_{13}	WRP	OPREQ	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	FS*
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	P X_1
2	X	X	X	1	1	1	1	0	1	0	0	0	0	0	1	X	X	X	E X_2
3	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	1	1	E X_3
4	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	E X_4
5	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	E X_5
6	X	X	X	X	1	1	0	1	0	0	X	X	X	X	X	X	X	X	E X_6
7	X	X	X	X	1	0	1	0	X	X	X	X	X	X	X	X	X	X	E X_7
8	X	X	X	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	PORT
9	X	X	X	1	1	1	0	1	0	1	0	X	X	X	X	X	X	X	RAM
10	X	X	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	ROM

DISABLE			PGA	XTL	R/C	EXT	1	2	3	4
			TIMING SOURCE			√		√		
ROM	RAM	PORT						CK Divide by		

*P = Port E = Enable

Table 8 SMI PROGRAM TABLE FOR HIGH PERFORMANCE MICROCOMPUTER SYSTEM

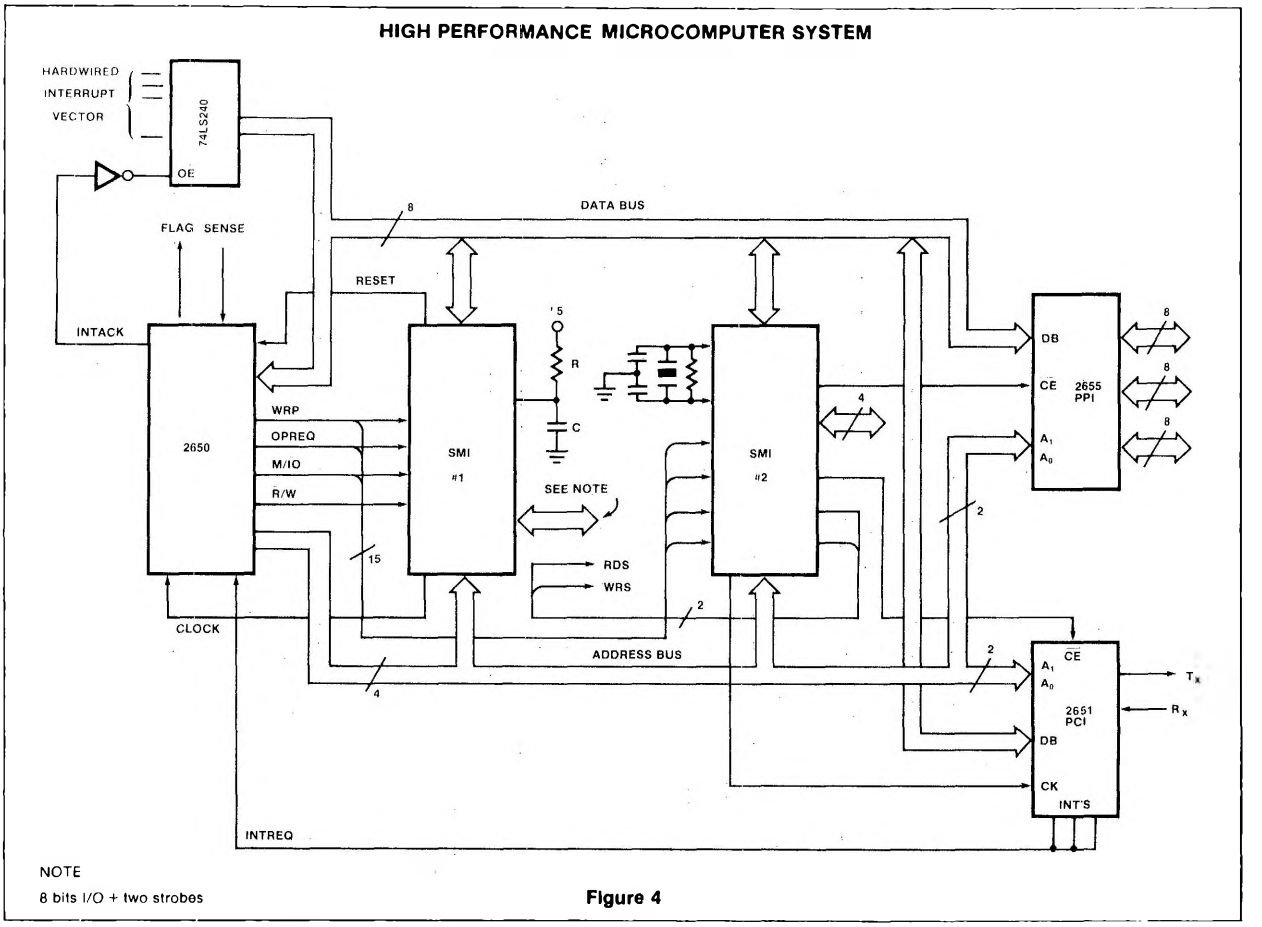


Figure 4

MICROCOMPUTER SYSTEM WITH MSI INPUT-OUTPUT

The system of Figure 5 incorporates MSI integrated circuits for input and output. It contains a total of 3k bytes of ROM/PROM, 384 bytes of RAM, six bits of SMI latch storage, one latching input port (74LS374), one gated input port (74LS240), one byte-oriented output port (74LS374), one bit-oriented output port (74LS259/93L34), two single bit inputs and two single bit outputs (one each from the SMI and the 2650). The SMI divides the external clock frequency by 1, 2, 3, or 4 and provides CLOCK and RESET outputs to the 2650. Six X pins are used for chip enables and two for data bits.

Included are system memory map (Table 9) and the SMI Program Table. The I/O device and the SMI port are all memory mapped; thus, the 2650 M/$\overline{IO}$ signal is not connected to the SMI.

WRP from the 2650 is connected to the SMI to control the two output ports:

1. When output-port-1's address and OPREQ are valid, the WRP input provides a gated chip enable on X_3. The trailing edge of this signal is used to clock 2650 data into the 74LS374.
2. One bit of 2650 data is gated into the 74LS259/93L34 addressable latch (output port 2) by means of X_2 which serves as the enable input. This signal is active when output port 2 has been selected. At the same time, three address bus lines select the latch to be written into.

	PIN	BYTES	ADDRESS
Internal ROM	—	2k	0000-07FF
External PROM (82S181)	X_7	1k	0800-0BFF
External RAM (2-2112's)	X_6	256	1400-14FF
Internal RAM	—	128	1500-157F
SMI Port	—	1	1A00
Input Port 1 (74LS374)	X_5	1	1A01
Input Port 2 (74LS240)	X_4	1	1A02
Output Port 1 (74LS374)	X_3	1	1A03
Output Port 2 (74LS259/93L34)	X_2	8	1A08 - 1A0F

Table 9 ADDRESS MAP FOR MSI I/O SYSTEM

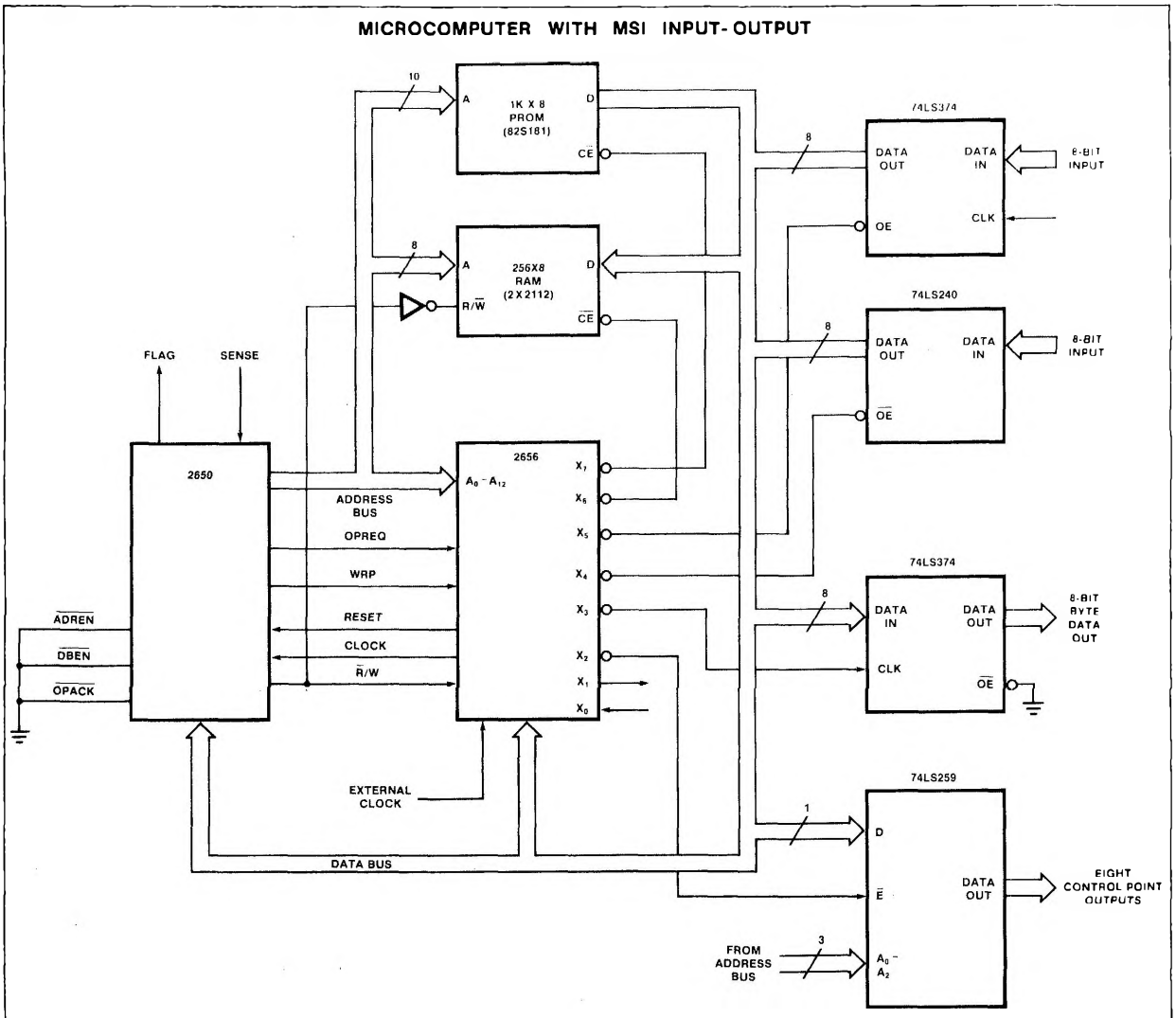

MICROCOMPUTER WITH MSI INPUT-OUTPUT
1K X 8 PROM (82S181)
256X8 RAM (2X2112)
2650
2656
74LS374
74LS240
74LS374
74LS259
DATA OUT
DATA IN
8-BIT INPUT
8-BIT BYTE DATA OUT
EIGHT CONTROL POINT OUTPUTS
FLAG
SENSE
ADDRESS BUS
OPREQ
WRP
RESET
CLOCK
R/W
ADREN
DBEN
OPACK
EXTERNAL CLOCK
DATA BUS
FROM ADDRESS BUS

Figure 5