signetics

FULLY DECODED 1024 AND 2048 STATIC READ-ONLY MEMORIES

METAL GATE MOS

2441
2451
2461
2462

DESCRIPTION

These Signetics devices are high speed, fully decoded, MOS static 1024 and 2048-bit read-only memories offering 128X8, 126X4, and 512X4 organizations.

Both single line and 3-bit binary coded chip select options, provide for wide versatility and economy of application. The devices interface directly with standard TTL/DTL logic circuits. Process technology is P-Channel enhancement mode.

FEATURES

- **128X8, 256X8, 256X4, 512X4 ORGANIZATIONS**
- **STATIC OPERATION - NO CLOCKS**
- **FULLY DECODED ADDRESS**
- **ACCESS TIME 950ns MAX.**
- **TTL/DTL COMPATIBILITY**
- **BARE DRAIN OUTPUT**
- **TWO CHIP SELECT OPTIONS:**
  - **SINGLE LINE**
  - **3-BIT BINARY CODED**
- **EBCDIC-ASCII CONVERSION (CM4030) TABLE IS CATALOG STANDARD, OTHER STANDARDS AVAILABLE**
- **+5, -12V POWER SUPPLIES**
- **STANDARD PINNING IN 16 AND 24 PIN CERAMIC DUAL IN-LINE PACKAGES**

APPLICATIONS

CODE CONVERSION
LOOK-UP TABLES
MICRO-PROGRAMMING
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION

SPECIAL FEATURES

Chip Select Options: Both the 2451 and 2461 may be specified with either single line chip select or a 3 line, 3-bit binary coded chip select. The coded chip select allows one-of-eight chip selection without external logic components for larger memory matrices. The 2441 and 2462 are pin limited to single line chip select.

Package Options: The 256X4 organization is available in *either* a 16-pin or 24-pin dual in-line package.

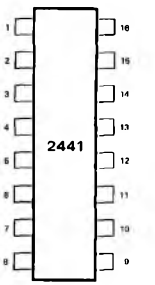
For a detailed listing of part numbers and options see the PART IDENTIFICATION TABLE.

CUSTOM ENCODING

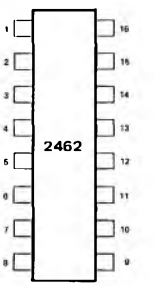
You may describe the particular option you desire in a booklet which will be provided by Signetics. Ask your local Signetics representative for a copy of "SIGNETICS 2400 SERIES STATIC READ-ONLY MEMORIES – MOS-ROM PROGRAMMING". The booklet contains a blank truth table and instructions for preparing punched data cards.

PIN CONFIGURATIONS (Top View)

I PACKAGE

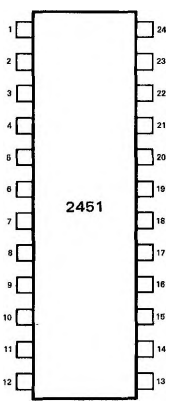


1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
16. V_{DD}
15. Address 4
14. Address 5
13. Address 6
12. Address 7
11. V_{GG}
10. Chip Enable
9. Address 8



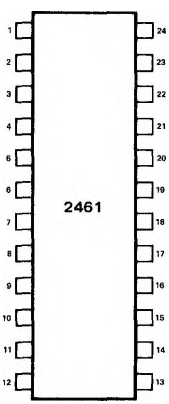
1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. V_{SS}
16. Address 4
15. Address 5
14. Address 6
13. Address 7
12. Address 8
11. V_{GG}, V_{DD}
10. Chip Enable
9. Address 9

Y PACKAGE



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. V_{GG}
16. Mode Control
15. Chip Enable
14. Address 8
13. No Connection

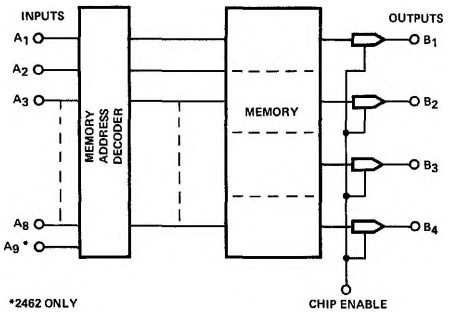
* No connection for single chip enable options.



1. Address 3
2. Address 2
3. Address 1
4. Output 1
5. Output 2
6. Output 3
7. Output 4
8. Output 5
9. Output 6
10. Output 7
11. Output 8
12. V_{SS}
24. V_{DD}
23. Chip Enable 3*
22. Chip Enable 2*
21. Address 4
20. Address 5
19. Address 6
18. Address 7
17. Address 8
16. V_{GG}
15. Mode Control
14. Chip Enable
13. Address 9

* No connection for single chip enable options.

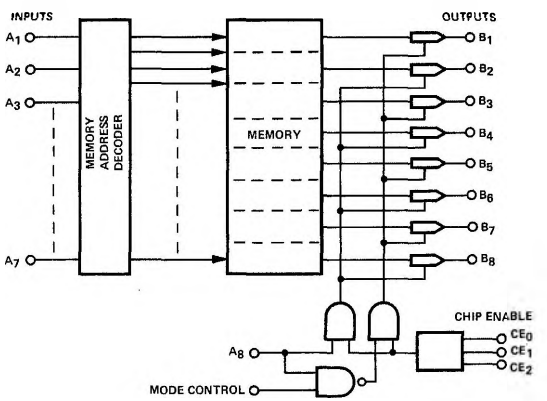
BLOCK DIAGRAMS



2441, 2462

OPERATING MODE

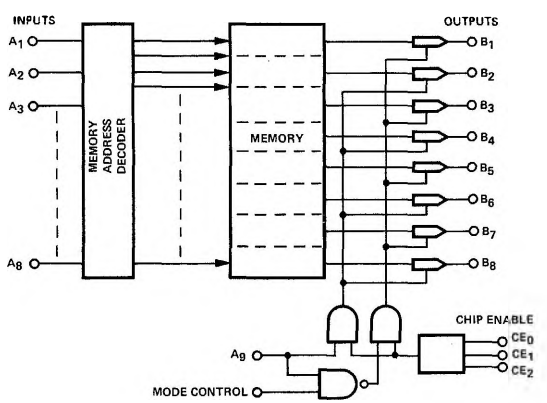
1. Logic "1" level enables outputs.



2451

OPERATING MODES

1. 128 x 8 ROM Connections
   Mode Control – Logic "0"
   A8 – Logic "1"
2. 256 x 4 ROM Connection
   Mode Control – Logic "1"
   A8 – Logic "0" Enables the odd (B1, B3, B5, B7) outputs.
   – Logic "1" Enables the even (B2, B4, B6, B8) outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.



2461

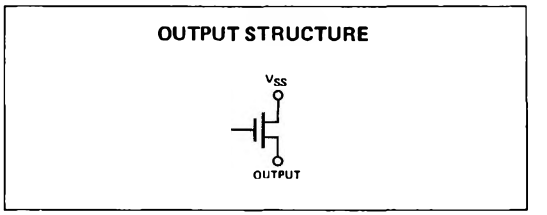
OPERATING MODES

1. 256 x 8 ROM Connection
   Mode Control – Logic "0"
   A9 – Logic "1"
2. 512 x 4 ROM Connection
   Mode Control – Logic "1"
   A9 – Logic "0" Enables the odd (B1, B3 . . B7) Outputs
   – Logic "1" Enables the even (B2, B4. . B8) Outputs
3. CE_0, CE_1, and CE_2 are AND'ed per customer instructions.

ABSOLUTE MAXIMUM RATINGS (1)

Operating Ambient Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2) ("Y" Package)	@70°C 1.14W
("I" Package)	@70°C 0.80W
V_{GG}(3)	−20 to +0.3
V_{DD}(3)	−15 to +0.3
Input Voltage (3,4)	−20 to +0.3

SCHEMATIC DIAGRAM



DC CHARACTERISTICS

T_A = −25°C to +70°C; V_{SS} = +5V ±5%; V_{DD} = V_{GG} = −12V ±5% unless otherwise noted (Notes: 8, 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Input Logic "0"	3			V	
V_{IH}	Input Logic "1"			0.8	V	
I_{SS}	V_{SS} Power Supply Current		14	20	mA	T_A = 25°C
I_{GG}	V_{GG} Power Supply Current			1	μA	Note 5, T_A = 25°C
I_{IH}	Input Leakage			1	μA	V_{IN} = −12V

AC CHARACTERISTICS

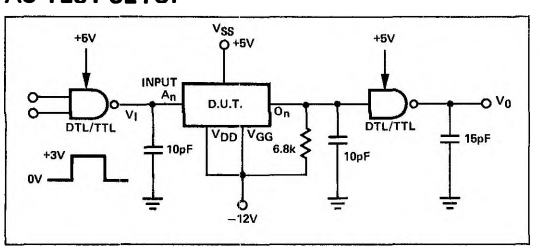
T_A = 25°C; V_{SS} = +5V ±5%; V_{DD} = V_{GG} = −12V ±5% unless otherwise noted (Notes 9, 10, 11, 12, 14)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0" MOS to TTL	+2.4			V	Note 6
V_{OH}	Output Logic "1"			+0.4	V	Note 6
t_{A1}	Access Time			750	ns	Note 13
t_{A0}	Access Time			950	ns	
C_{IN}	Input Capacitance		5		pF	Note 7, f = 1 MHz, V_{IN} = 0

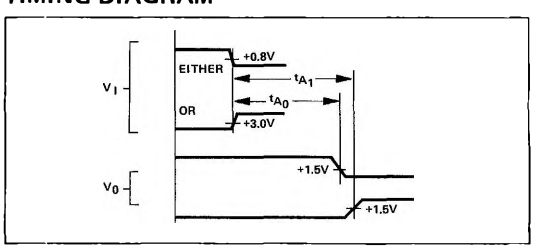
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only. Operation of the device at those or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operation at elevated temperatures, the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 70°C/W junction to ambient for the "Y" package. The "I" package is derated based on 100°C/W junction to ambient.
3. These voltages are referenced to network ground terminal (V_{SS}).
4. All inputs are protected against damage by static charge.
5. The V_{GG} supply may be clocked to reduce device power without affecting access time.
6. 6.8kΩ to V_{GG} plus 1 standard TTL gate input.
7. Capacitance measured on lot sample basis only.
8. Parameter valid over operating temperature range unless otherwise specified.
9. All voltage measurements referenced to ground.
10. Manufacturer reserves the right to make design changes and process improvements.
11. Typical values are at 25°C and nominal supply voltages.
12. Negative logic definition is employed for this device. I.e., more negative level is logic "1", most positive level is logic "0".
13. For bare drain devices, T_{A1} is primarily a function of the time constant of the load capacitance and external load resistor ($t_{A1} \doteq 4R_L C_L$ +50 ns).
14. CAUTION: These devices will be permanently damaged if reversed in board or socket.

AC TEST SETUP



TIMING DIAGRAM



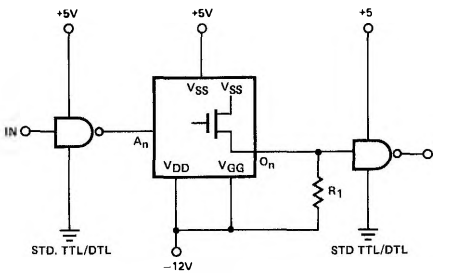
PART IDENTIFICATION TABLE

PART	ORGANIZATION	PACKAGE	OUTPUTS
N2441I	256 x 4	16-pin Cer. DIP	Bare Drain
N2451Y	128 x 8 or 256 x 4	24-pin Cer. DIP	Bare Drain
N2461Y/ CM 4030	256 x 8 (EBCDIC-ASCII) *	24-pin Cer. DIP	Bare Drain
N2461Y	256 x 8 or 512 x 4	24-pin Cer. DIP	Bare Drain
N2462I	512 x 4	16-pin Cer. DIP	Bare Drain

* Demonstrator

APPLICATIONS

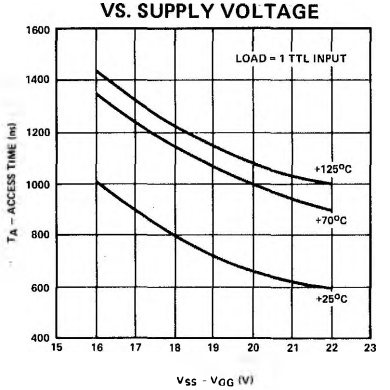
MOS-TTL INTERFACING



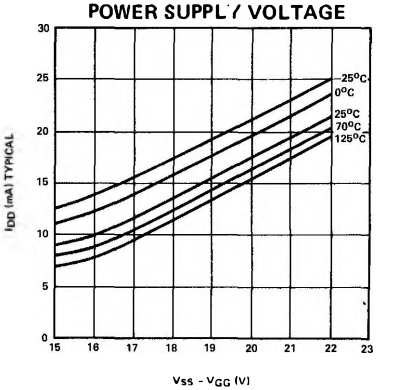
R_1 = 6.8k for a standard TTL (I_O IN = 1.6mA)

CHARACTERISTIC CURVES

TYPICAL ACCESS TIME VS. SUPPLY VOLTAGE



TYPICAL POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE



NOTE: For typical curves, V_{SS} = 0V.

NOTE: Blanks are logic 1's.

CM 4030 TRUTH TABLE

EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EDCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7	EBCDIC WORD #	ASCII CODE BIT NUMBER 1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	65								130	0	1	0	0	0	1	1	195	1	1	0	0	0	0	1
1	1	0	0	0	0	0	0	66								131	1	1	0	0	0	1	1	196	0	0	1	0	0	0	1
2	0	1	0	0	0	0	0	67								132	0	0	1	0	0	1	1	197	1	0	1	0	0	0	1
3	1	1	0	0	0	0	0	68								133	1	0	1	0	0	1	1	198	0	1	1	0	0	0	1
4								69								134	0	1	1	0	0	1	1	199	1	1	1	0	0	0	1
5	0	1	1	0	0	0	0	70								135	1	1	1	0	0	1	1	200	0	0	0	1	0	0	1
6								71								136	0	0	0	1	0	1	1	201	1	0	0	1	0	0	1
7	1	1	1	1	1	1	1	72								137	1	0	0	1	0	1	1	202							
8								73								138								203							
9								74								139								204							
10								75	0	1	1	1	0	1	0	140								205							
11	1	1	0	1	0	0	0	76	0	0	1	1	1	1	0	141								206							
12	0	0	1	1	0	0	0	77	0	0	0	1	0	1	0	142								207							
13	1	0	1	1	0	0	0	78	1	1	0	1	0	1	0	143								208							
14	0	1	1	1	0	0	0	79	0	0	1	1	1	1	1	144								209	0	1	0	1	0	0	1
15	1	1	1	1	0	0	0	80	0	1	1	0	0	1	0	145	0	1	0	1	0	1	1	210	1	1	0	1	0	0	1
16	0	0	0	0	1	0	0	81								146	1	1	0	1	0	1	1	211	1	1	1	1	1	1	1
17	1	0	0	0	1	0	0	82								147	0	0	1	1	0	1	1	212	1	0	1	1	0	0	1
18	0	1	0	0	1	0	0	83								148	1	0	1	1	0	1	1	213	0	1	1	1	0	0	1
19	1	1	0	0	1	0	0	84								149	0	1	1	1	0	1	1	214	1	1	1	1	0	0	1
20								85								150	1	1	1	1	0	1	1	215	0	0	0	0	1	0	1
21								86								151	0	0	0	0	1	1	1	216	1	0	0	0	1	0	1
22	0	0	0	1	0	0	0	87								152	1	0	0	0	1	1	1	217	0	1	0	0	1	0	1
23								88								153	0	1	0	0	1	1	1	218							
24	0	0	0	1	1	0	0	89								154								219							
25	1	0	0	1	1	0	0	90	1	0	0	0	0	1	0	155								220							
26								91	0	0	1	0	0	1	0	156								221							
27								92	0	1	0	1	0	1	0	157								222							
28	0	0	1	1	1	0	0	93	1	0	0	1	0	1	0	158								223							
29	1	0	1	1	1	0	0	94	1	1	0	1	1	1	0	159								224							
30	0	1	1	1	1	0	0	95								160								225							
31	1	1	1	1	1	0	0	96	1	0	1	1	0	1	0	161								226	1	1	0	0	1	0	1
32								97	1	1	1	1	0	1	0	162	1	1	0	0	1	1	1	227	0	0	1	0	1	0	1
33								98								163	0	0	1	0	1	1	1	228	1	0	1	0	1	0	1
34								99								164	1	0	1	0	1	1	1	229	0	1	1	0	1	0	1
35								100								165	0	1	1	0	1	1	1	230	1	1	1	0	1	0	1
36								101								166	1	1	1	0	1	1	1	231	0	0	0	1	1	0	1
37	0	1	0	1	0	0	0	102								167	0	0	0	1	1	1	1	232	1	0	0	1	1	0	1
38	1	1	1	0	1	0	0	103								168	1	0	0	1	1	1	1	233	0	1	0	1	1	0	1
39	1	1	0	1	1	0	0	104								169	0	1	0	1	1	1	1	234							
40								105								170								235							
41								106								171								236							
42								107	0	0	1	1	0	1	0	172								237							
43								108	1	0	1	0	0	1	0	173								238							
44								109	1	1	1	1	1	0	1	174								239							
45	1	0	1	0	0	0	0	110	0	1	1	1	1	1	0	175								240	0	0	0	0	1	1	0
46	0	1	1	0	0	0	0	111	1	1	1	1	1	1	0	176								241	1	0	0	0	1	1	0
47	1	1	1	0	0	0	0	112								177								242	0	1	0	0	1	1	0
48								113								178								243	1	1	0	0	1	1	0
49								114								179								244	0	0	1	0	1	1	0
50	0	1	1	0	1	0	0	115								180								245	1	0	1	0	1	1	0
51								116								181								246	0	1	1	0	1	1	0
52								117								182								247	1	1	1	0	1	1	0
53								118								183								248	0	0	0	1	1	1	0
54								119								184								249	1	0	0	1	1	1	0
55	0	0	1	0	0	0	0	120								185								250							
56								121								186								251							
57								122	0	1	0	1	1	1	0	187								252							
58								123	1	1	0	0	0	1	0	188								253							
59								124	0	0	0	0	0	0	1	189								254							
60	0	0	1	0	1	0	0	125	1	1	1	0	0	1	0	190								255							
61	1	0	1	0	1	0	0	126	1	0	1	1	1	1	0	191															
62								127	0	1	0	0	0	1	0	192															
63	0	1	0	1	1	0	0	128	0	1	0	0	0	1	0	193	1	0	0	0	0	0	1								
64	0	0	0	0	0	1	0	129	1	0	0	0	0	1	1	194	0	1	0	0	0	0	1								

EXERPT FROM SOFTWARE PACKAGE (CARD FORMAT)

CARD 1

COLUMN	DATA
1-8	STARTING AT COLUMN 1 PUNCH "CODED" OR "SINGLE"
9-11*	IF "CODED" PUNCH THE BINARY CODE CHIP SELECT (i.e. 101) IF "SINGLE" LEAVE BLANK
12	LEAVE BLANK
13-17	PUNCH THE ROM ORGANIZATION DESIRED (i.e. 8 X 256, 4 X 512, ETC.
18	BLANK
19-21	PUNCH MOS FOR AN MOS OUTPUT PUNCH TTL FOR A TTL OUTPUT (BARE DRAIN)
22-27	BLANK
28-33	PUNCH THE BASIC DEVICE TYPE DESIRED (i.e. N2416, N2425Y, ETC.
34-80	COMMENTS PUNCHED HERE WILL APPEAR AS THE TITLE ON THE TRUTH TABLE THIS SHOULD INCLUDE CUSTOMER PART IDENTIFICATION

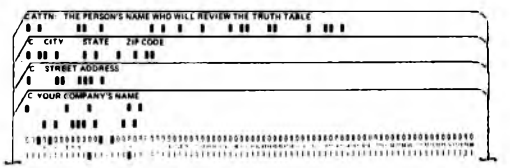
*CE_3, CE_2 and CE_1 respectively

CARD 2 THROUGH 129 (8 X 128 Organization)
2 THROUGH 256 (8 X 256 Organization)

EACH CARD SPECIFIES THE OUTPUT OF ONE 8-BIT WORD IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS FOR THAT WORD IS PUNCHED IN COLUMNS 78, 79 AND 80.

COLUMNS	DATA
1-8	PUNCH OUTPUTS B1 THROUGH B8 IN COLUMNS ONE THROUGH EIGHT RESPECTIVELY
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS WHICH CORRESPONDS TO THE OUTPUTS PUNCHED IN COLUMNS 1-8 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

EXAMPLE:
ADDRESS CARDS



CARDS 2 THROUGH 129 (4 X 256 Organization only)

EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHED IN COLUMNS 78, 79, AND 80.

COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-255
5-8	PUNCH OUTPUT FOR WORDS 256-511
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS OF THE WORD CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

CARDS 2 THROUGH 2574 (4 X 512 Organization only)

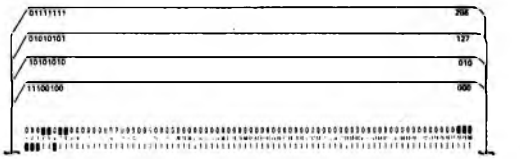
EACH CARD SPECIFIES THE OUTPUT OF TWO 4-BIT WORDS IN COLUMNS 1 THROUGH 8. THE DECIMAL EQUIVALENT OF THE BINARY CODED INPUT ADDRESS IS PUNCHES IN COLUMNS 78, 79, AND 80.

COLUMN	DATA
1-4	PUNCH OUTPUT FOR WORDS 0-127
5-8	PUNCH OUTPUT FOR WORDS 128-255
9-77	LEAVE BLANK
78-80	PUNCH DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS CORRESPONDING TO THE OUTPUTS PUNCHED IN COLUMNS 1-4 COLUMN 78 HUNDREDS DIGIT COLUMN 79 TENS DIGIT COLUMN 80 UNITS DIGIT

EXAMPLE
CARD 1

THE ABOVE SPECIFIES A "CODED" ROM WITH THE BINARY CODED CHIP SELECT "101" ORGANIZED 8 X 256 WITH TTL OUTPUTS (BARE DRAIN). THE BASIC DEVICE TYPE IS A N2436Y ("Y" INDICATES A 24 PIN CERAMIC DIP. N INDICATES TEMPERATURE RANGE: -25 C – +70 C).

EXAMPLE
CARDS 2-129 AND CARDS 2-257



- OUTPUTS B1 THROUGH B8 ARE IN COLUMNS 1 THROUGH 8 RESPECTIVELY.
- DECIMAL EQUIVALENT OF BINARY CODED INPUT ADDRESS IS IN COLUMNS 78, 79, AND 80.
- FOR 8 X 128 AND 8 X 256 ORGANIZATIONS – OUTPUTS ARE B1 THROUGH B8 RESPECTIVELY
- FOR 4 X 512 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 256 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 266 OUTPUTS B5 THROUGH B8 RESPECTIVELY

ETC.

- FOR 4 X 256 ORGANIZATION:

DATA CARD 0	WORD 000 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 128 OUTPUTS B5 THROUGH B8 RESPECTIVELY
DATA CARD 10	WORD 010 OUTPUTS B1 THROUGH B4 RESPECTIVELY WORD 138 OUTPUTS B5 THROUGH B8 RESPECTIVELY