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Lumped constant

- Low profile
- TTL and DTL compatible
- Low distortion and low attenuation
- High reliability
- Auto insertable

STANDARD PIN-OUT (CODE E)

description

The 11A series of Delay Lines are constructed from passive, lumped-constant components forming a delay line ladder. Up to 10 equally spaced delay taps are available in a low profile 14 pin dual-in-line package particularly suitable for high-density board designs. No termination resistor is included which allows for series connection of a number of delay lines for unequal tap designs. Direct drive from TTL and DTL is easily achieved with a minimum of design know-how.

absolute maximum ratings over operating free-air temperature range

Temperature coefficient of delay
Operating free-air temperature range
Storage temperature range
Operating voltage
Characteristic impedance Zo
Distortion
Insulation resistance
Dielectric strength
Total delay/rise time ratio
Min. pulse width as % of total delay
Input pulse repetition rate PRR
Lead temperature1.5mm from case for 10 seconds

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delay characteristics Ta = 25C, input test pulse voltage 3V, pulse width 3 x total delay, rise time 3ns, delay line termination \pm 1% of nominal Zo.

delay tolerance from input to tap ± 2 ns or ± 5 % whichever is greater

PART No. (1)	TOTAL DELAY (ns)±5% (2)	TAP TO TAP DELAY (ns) ±10% (3)	RISE TIME (ns) max.	ATTENUATION (%) MAX.
11ACB10012E 11ACB20012E 11ACB30012E 11ACB40012E 11ACB50012E	10 20 30 40 50	1 2 3 4 5	3 4.5 6 7 8.5	5555
11ACB60012E 11ACB75012E 11ACB10112E 11ACB12112E 11ACB12112E 11ACB15112E	60 75 100 120 150	6 7.5 10 12 15	10 12.5 17 20 25	5 5 5 5 5 5
11ACB18112E 11ACB20112E 11ACB25112E 11ACB30112E 11ACB30112E 11ACB50112E	180 200 250 300 500	18 20 25 30 50	30 34 42 50 85	5 5 5 5 8

11A Series 10 Tap 14 Pin DIL Package style C

(1) For 100Ω impedance parts
(2) or ±2ns whichever is greater,
(3) or ±1ns whichever is greater,

Note:Other impedances and pinouts are available to special order. Delays measured between 50% points on leading edges of input and output signals.

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