

DUAL 3-INPUT 10110 3-OUTPUT OR GATE

10110B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



DESCRIPTION

The 10110 is a dual high speed 3-input 3-output OR gate. The 10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire."OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the 10110 particularly useful in clock distribution applications where minimum clock skew is desired.

FEATURES

- FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)
- POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS INTERNAL 50 k Ω PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIA-TIONS: VEE = -5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

TEMPERATURE RANGE

• -30 to +85°C Operating Ambient

PACKAGE TYPE

- B: 16-Pin Silicone DIP
- F: 16-Pin CERDIP

TEST VOLTAGE VALUES

ELECTRICAL CHARACTERISTICS

| (At Listed Voltages and Ambient Temperatures). | | | | | | | | | ngerature | VIH mex | VIL min | VIHA min | VILA mex | VEE | | |
|--|---------|----------------------|-------------------|--------|---------|-----|--------|--------|-----------|---------|--|----------|----------|-----------|--------|---------|
| | | | | | | | | | | -30° C | -0.890 | -1.890 | -1.205 | -1.500 | -5.2 | |
| +26 | | | | | | | | | | | -0.810 | -1.850 | 0 -1.105 | -1.475 | -5.2 | |
| _ | | | | | | | | | | +85°C | -0.700 | -1.825 | -1.035 | -1.440 | -5.2 | |
| Characteristic | Symbol | Pin Under Test | 10110 Test Limits | | | | | | | | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: | | | | | |
| | | | -30°C | | | | +85°C | | | , | T T | | | r | (Vcc) | |
| | | | Min ' | Max | Min | Тур | Мак | Min | Max | Unit | VIH mex | VIL min | VIHA min | VILA max | VEE | Gnd |
| Power Supply Drain Current | 1E | 8 | 2 | 1 | - | - | 38 | - | - | mAde | - | - | - | - | 8 | 1,15,16 |
| Input Current | linH | 5,6,7 | - | 1 | ÷. | - | 435 | | - | #Adc | | - | - | - | 8 | 1,15,16 |
| | link | 5,6,7 | | 1 | 0.5 | - | - | Ţ | - | µAdc | - | | - | - | 8 | 1,15,16 |
| Logic "1" Output Voltage | VOH | 2 | -1.060 | 0 890 | -0.960 | - | 0 810 | -0.890 | -0.700 | Vdc | 5 | ~ | - | - | 8 | 1,16,16 |
| | | 3 | - 1.060 | -0 890 | -0 960 | - | -0.810 | -0.890 | -0.700 | Vric | 6 | - | - | - | 8 | 1,15,16 |
| | | 4 | -1.060 | -0.890 | -0.960 | - | -0.810 | -0.890 | -0.700 | Vdc | 7 | | - | - | 8 | 1,15,16 |
| Lagic "O" Output Voltege | VOL | 2 | -1.890 | -1.675 | -1.860 | - | -1.650 | -1.825 | -1.615 | Vdc | - | 5 | 1 | - | 8 | 1,15,16 |
| | | 3 | -1.890 | -1.675 | -1.850 | - | -1.660 | -1.825 | -1.615 | Vdc | - | 6 | | - | 8 | 1,15,16 |
| | | 4 | -1.890 | -1.675 | -1.850 | - | -1.650 | -1.825 | -1.615 | Vdc | - | 7 | | - | 8 | 1,16,16 |
| Logic "1" Threshold Voltage | VOHA | 2 | -1.080 | - | 0.980 | | - | -0.910 | - | Vdc | | - | 5 | - | 8 | 1,15,16 |
| | | 3 | -1.080 | - | -0.980 | - | - | -0.910 | - | Vdc | | | 6 | - | 8 | 1,15,16 |
| | | 4 | -1.080 | - | -0.980 | - | - | -0.910 | - | Vdc | - | ~ | 7 | - | 8 | 1,16,16 |
| Logic "O" Threshold Voltage | VOLA | 2 | - | -1.655 | - | 0 | -1.630 | - | -1.595 | Vdc | | < H) | | 5 | 8 | 1,15,16 |
| | 100.000 | 3 | | -1.655 | | | ~1.630 | - | -1.595 | Vdc | - | | - | 6 | 8 | 1,15,16 |
| | | 4 | - | -1.655 | - | - | -1.630 | - | -1.595 | Vdc | - E | | - | 7 | 8 | 1,16,16 |
| Switching Times ** (50-ohm load) | | | 199 | | | | 1.0 | | | | | | Pulse In | Pulse Out | -3.2 V | +2.0 V |
| Propagation Datay | 15+ 2+ | 2 | 1.4 | 3.5 | 1.4 | 2.4 | 3.5 | 1.5 | 3.8 | ns | - | | 5 | 2 | 8 | 1,15,16 |
| | 15 . 2- | 2 | | 1 | 1 | | | | | | - | - | 1 | 2 | | |
| | 15+ 3+ | 3 | | | | | | | | | 5 m . | - | | 3 | | |
| | 15-3- | 3 | | | | | | | | | | - | | 3 | | |
| | 15+ 4+ | 4 | | | 1 mar 1 | | | | | | - | 100 | | 4 | | |
| | 16-4- | 4 | | | | | | | | | dia. | - | | 4 | | |
| File Time (20% to 80%) | 124 | 2 | 1.0 | | 1.1 | 2.2 | | 1.2 | | | - | - | 1 | 2 | | |
| | 134 | 3 | | | | | | | | | - | - | | 3 | | |
| | 14. | 4 | | | | | | | | | - | - | | 4 | | |
| Fall Time (20% to 80%) | 12_ | 2 | | | | | | | | | - | - | | 2 | | |
| | 13. | 3 | | | | | | | | | ~ | <u></u> | | 3 | | |
| | ta_ | 4 | | | 1 | T | 1 | 1 | 1 | 1 | | - | | 4 | | - T |
| | | | | | | | | | | | | | | | | 4 |

*Individually test each input using the pin connections shown.

** Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- 1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm, Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4Inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- 3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- 4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.