

10109B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

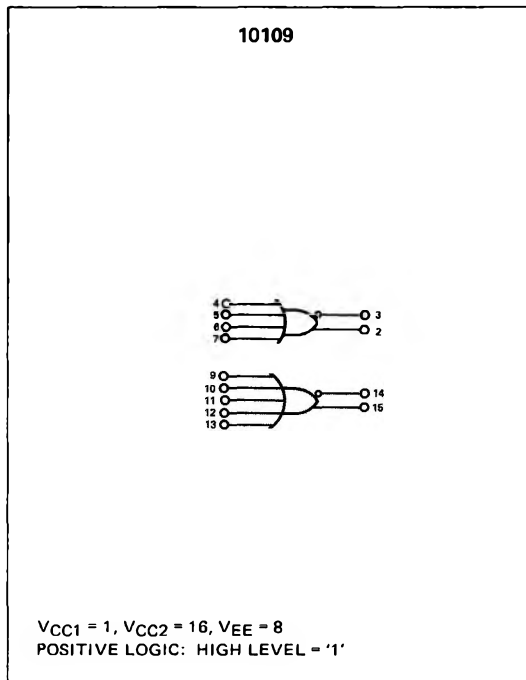
DESCRIPTION

The 10109 is a high speed 4-input OR/NOR and 5-input OR/NOR dual gate. All inputs are terminated with a 50 kΩ resistor to V_{EE} which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10109 is optimized for high performance logic applications. The 10109 has complementary outputs.

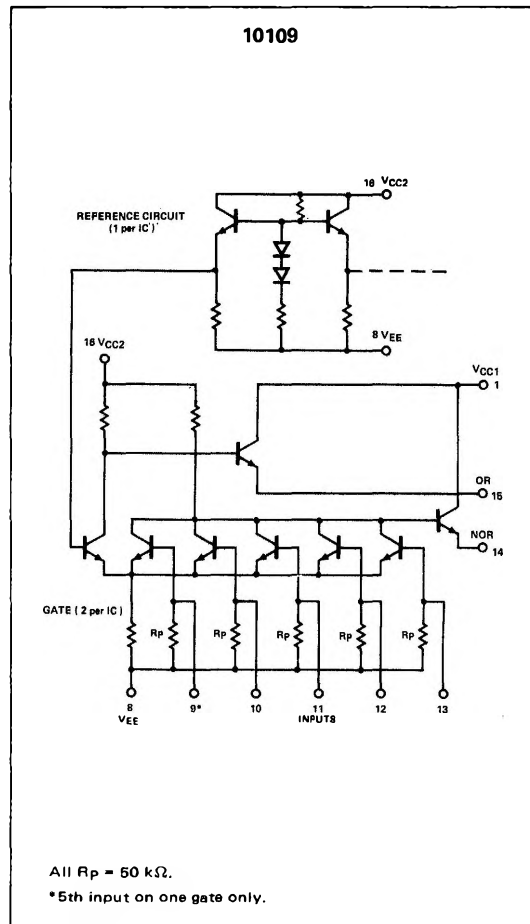
FEATURES

- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 50 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
— CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS — INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = -5.2 V ±5% RECOMMENDED
- COMPLEMENTARY OR/NOR OUTPUTS
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



TEMPERATURE RANGE

- -30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP

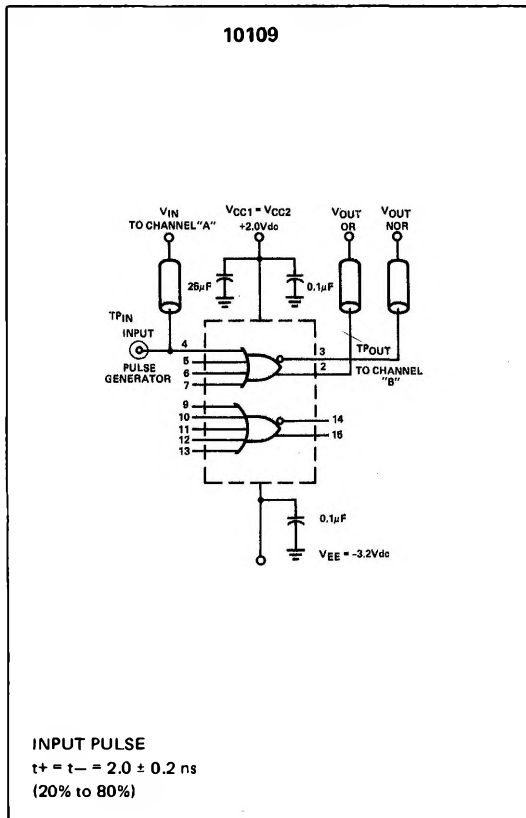
F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

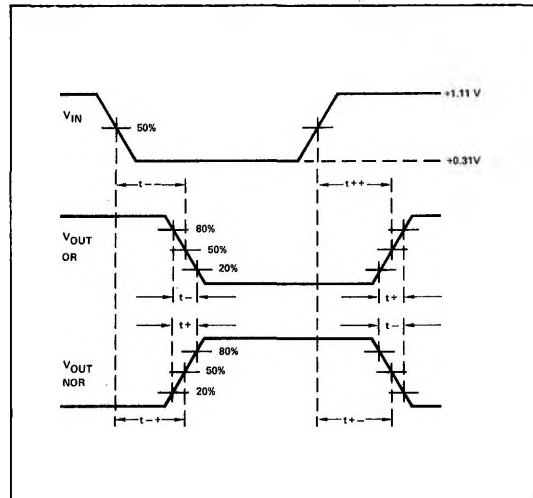
Characteristic	Symbol	Pin Under Test	10109 Test Limits								TEST VOLTAGE VALUES					Unit	V _{CC} Gnd
			-30°C		+25°C		+85°C		(Volts)								
			Min	Max	Min	Max	Min	Max	V _{IH} max	V _{IL} min	V _{IHA} min	V _{IHA} max	V _{EE}				
Power Supply Drain Current	I _E	8	—	—	—	10	14	—	—	—	—	—	—	—	—	8	1,16
Input Current	I _{IN}	4	—	—	—	—	265	—	—	—	—	—	—	—	—	8	1,16
	I _{INL}	4	—	0.5	—	—	—	—	—	—	—	—	—	—	—	8	1,16
High Output Voltage	V _{OH}	2	-1.080	-0.890	-0.860	—	-0.810	-0.890	-0.700	—	—	—	—	—	—	8	1,16
		3	-1.080	-0.890	-0.860	—	-0.810	-0.890	-0.700	—	—	—	—	—	—	8	1,16
Low Output Voltage	V _{OL}	2	-1.890	-1.676	-1.850	—	-1.650	-1.826	-1.616	—	—	—	—	—	—	8	1,16
		3	-1.890	-1.676	-1.850	—	-1.650	-1.826	-1.616	—	—	—	—	—	—	8	1,16
High Threshold Voltage	V _{OHA}	2	-1.080	—	-0.980	—	—	-0.910	—	—	—	—	—	—	—	8	1,16
		3	-1.080	—	-0.980	—	—	-0.910	—	—	—	—	—	—	—	8	1,16
Low Threshold Voltage	V _{OLA}	2	—	-1.866	—	—	-1.830	—	-1.666	—	—	—	—	—	—	8	1,16
		3	—	-1.866	—	—	-1.830	—	-1.666	—	—	—	—	—	—	8	1,16
Switching Times* (60-ohm load)																	
Propagation Delay	14+ 2+	2	1.0	3.1	1.0	2.0	2.8	1.0	3.3	ns	—	—	4	2	8	1,16	
	14- 2-	2	↓	↓	↓	↓	↓	↓	↓	—	—	—	2	2	—	—	
	14+ 3-	3	↓	↓	↓	↓	↓	↓	↓	—	—	—	3	3	—	—	
	14- 3+	3	↓	↓	↓	↓	↓	↓	↓	—	—	—	3	3	—	—	
Rise Time (20% to 80%)	12+	2	1.1	3.6	1.1	—	3.3	1.1	3.7	—	—	—	2	2	—	—	
	13+	3	↓	↓	↓	↓	↓	↓	↓	—	—	—	3	3	—	—	
Fall Time (20% to 80%)	12-	2	↓	↓	↓	↓	↓	↓	↓	—	—	—	2	2	—	—	
	13-	3	↓	↓	↓	↓	↓	↓	↓	—	—	—	3	3	—	—	

*Unused outputs connected to a 60-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.