FAIRCHILD SEMICONDUCTOR™

July 1989
Revised August 2000

100355
Low Power Quad Multiplexer/Latch

General Description

The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

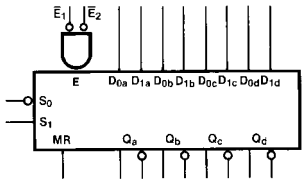
- Greater than 40% power reduction of the 100155
- 2000V ESD protection
- Pin/function compatible with 100155
- Voltage compensated operating range = –4.2V to –5.7V
- Available to industrial grade temperature range

Ordering Code:

Order Number	Package Number	Package Description
100355PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100355QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100355QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

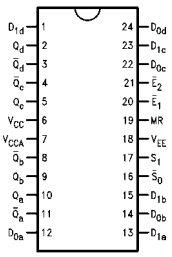


Pin Descriptions

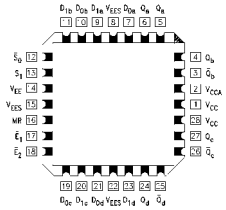
Pin Names	Description
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



28-Pin PLCC



Operating Mode Table

Controls				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched (Note 1)
X	H	X	X	Latched (Note 1)
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

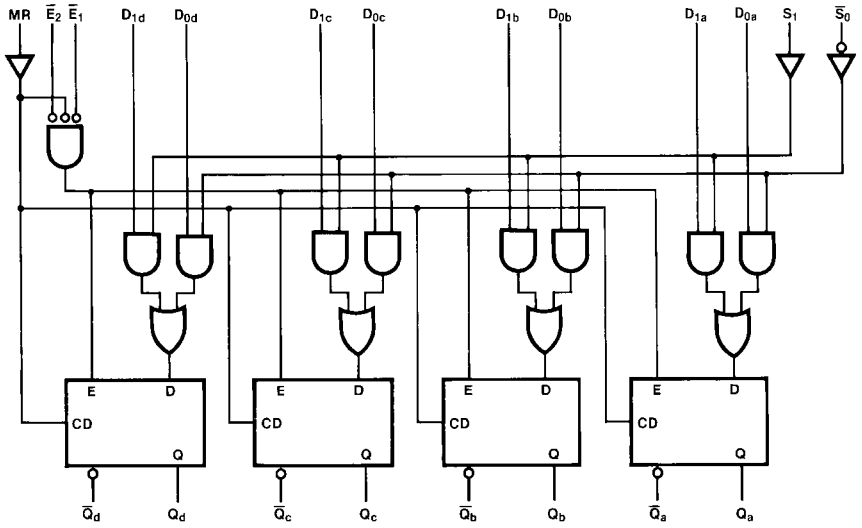
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Note 1: Stores data present before $\overline{E}$ went HIGH

Truth Table

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched (Note 1)	
L	X	H	X	X	X	X	Latched (Note 1)	

Logic Diagram



Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 4)

V_{EE} = −4.2V to −5.7V, $V_{CC} = V_{CCA}$ = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	$V_{IN} = V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	$V_{IN} = V_{IH\ (Min)}$	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50			µA	$V_{IN} = V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current						
	$\overline{S}_0$, S_1			220	µA	$V_{IN} = V_{IH\ (Max)}$	
	$\overline{E}_1$, $\overline{E}_2$			350			
	D_{na}–D_{nd}			340			
	MR			430			
I_{EE}	Power Supply Current	−87		−40	mA	Inputs Open	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)
DIP AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.90	0.60	1.90	0.70	2.00	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.60	1.00	2.60	1.20	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	2.00	0.80	2.00	0.80	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.30	0.80	2.30	0.80	2.30	ns	Figures 1, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.40	0.60	1.40	0.60	1.40	ns	Figures 1, 2
t_S	Setup Time								
	D_{na}–D_{nd}	0.90		0.90		0.90		ns	Figure 4
	$\overline{S}_0$, S_1	1.70		1.70		1.70			
	MR (Release Time)	1.50		1.50		1.50			Figure 3
t_H	Hold Time								
	D_{na}–D_{nd}	0.40		0.40		0.40		ns	Figure 4
	$\overline{S}_0$, S_1	0.00		0.00		0.00			
t_{PW} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	Figure 2
t_{PW} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3

Commercial Version (Continued)
PLCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	Figures 1, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.30	0.60	1.30	0.60	1.30	ns	Figures 1, 2
t_S	Setup Time							ns	
	D_{na}–D_{nd}	0.80		0.80		0.80			Figure 4
	$\overline{S}_0$, S_1	1.60		1.60		1.60			
	MR (Release Time)	1.40		1.40		1.40			Figure 3
t_H	Hold Time							ns	
	D_{na}–D_{nd}	0.30		0.30		0.30			Figure 4
	$\overline{S}_0$, S_1	−0.10		−0.10		−0.10			
t_{PW} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	Figure 2
t_{PW} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PLCC only (Note 5)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PLCC only (Note 5)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PLCC only (Note 5)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		270		270		270	ps	PLCC only (Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PLCC DC Electrical Characteristics (Note 6)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH\ (Min)}$	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	1830	1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current							
	$\overline{S}_0$, S_1		300		220	µA	V_{IN} = $V_{IH\ (Max)}$	
	$\overline{E}_1$, $\overline{E}_2$		350		350			
	D_{na}–D_{nd}		340		340			
	MR		430		430			
I_{EE}	Power Supply Current	−87	−40	−87	−40	mA	Inputs Open	

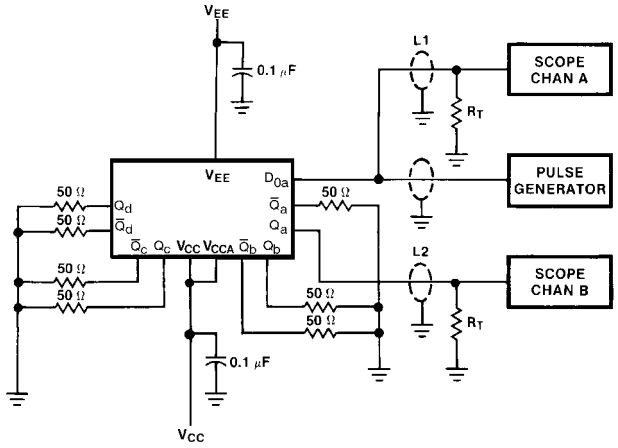
Note 6: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	Figures 1, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.60	1.30	0.60	1.30	ns	Figures 1, 2
t_S	Setup Time								
	D_{na}–D_{nd}	0.90		0.80		0.80		ns	Figure 4
	$\overline{S}_0$, S_1	2.40		1.60		1.60			
	MR (Release Time)	1.50		1.40		1.40			Figure 3
t_H	Hold Time								
	D_{na}–D_{nd}	0.40		0.30		0.30		ns	Figure 4
	$\overline{S}_0$, S_1	0.00		−0.10		−0.10			
t_{PW} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	Figure 2
t_{PW} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3

Test Circuit



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Switching Waveforms

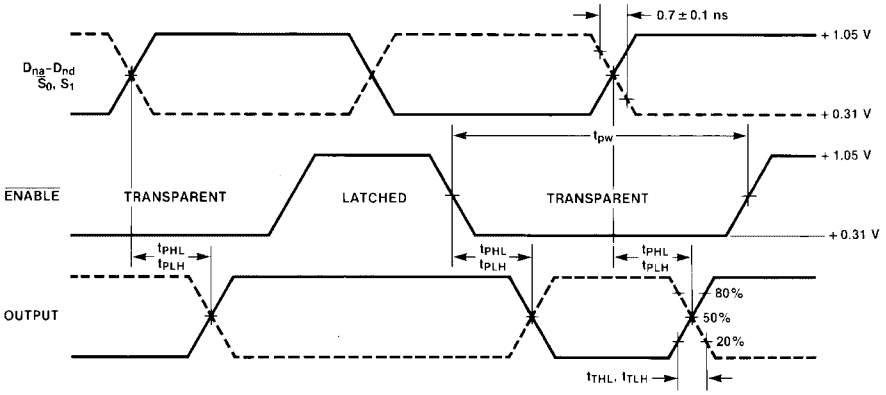


FIGURE 2. Enable Timing

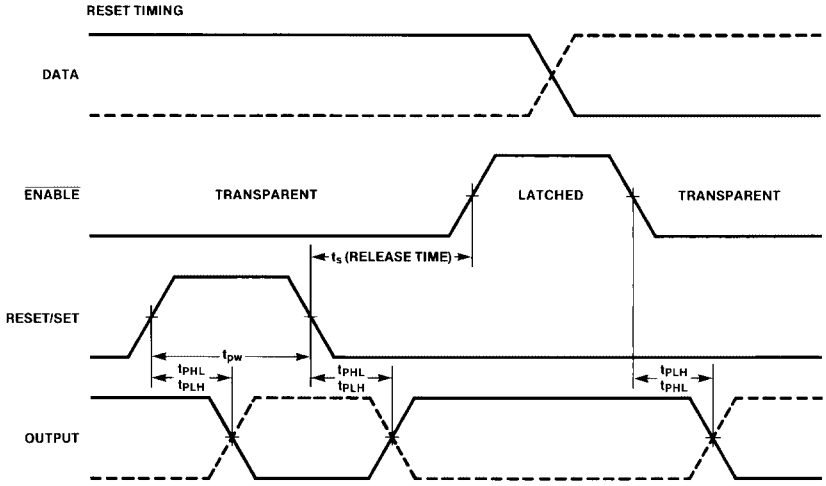
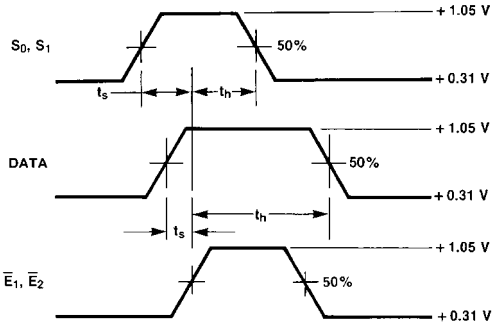


FIGURE 3. Reset Timing



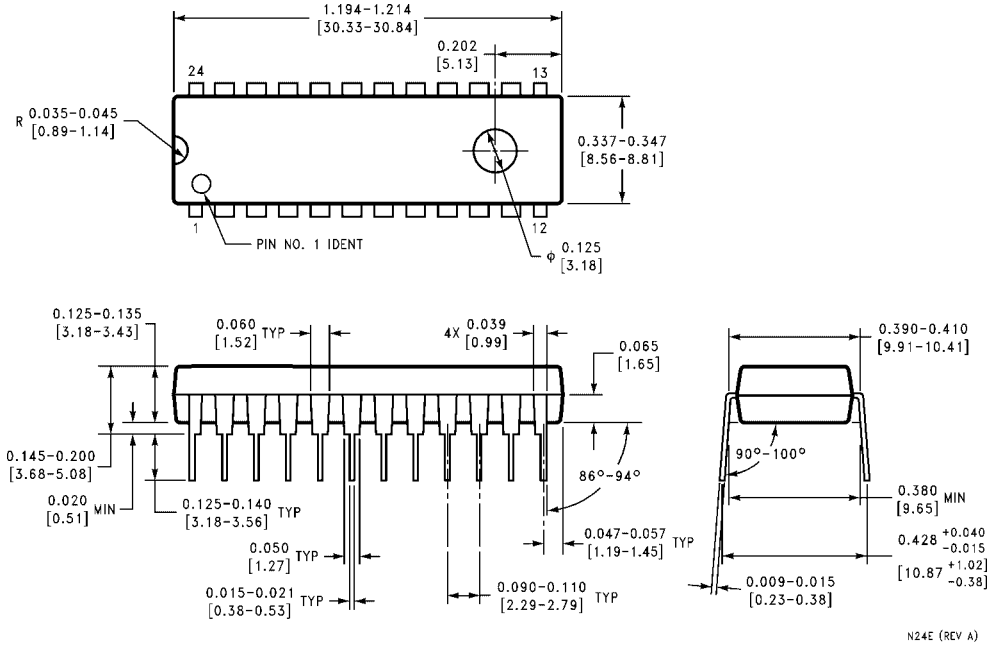
Notes:

t_S is the minimum time before the transition of the enable that information must be present at the data input.

t_H is the minimum time after the transition of the enable that information must remain unchanged at the data input.

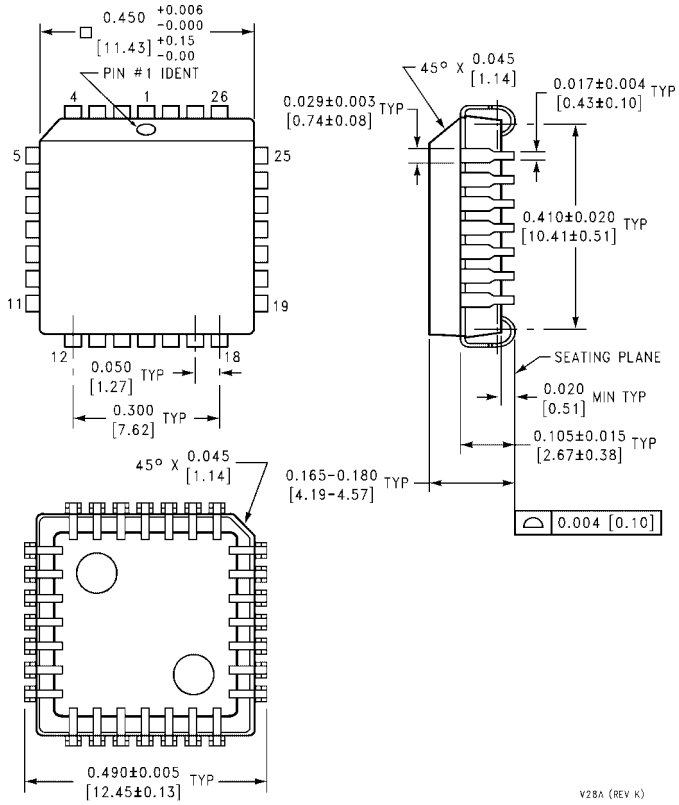
FIGURE 4. Data Setup and Hold Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A