# 100331

100331 Low Power Triple D Flip-Flop



Literature Number: SNOS116



August 1998

## 100331

# Low Power Triple D Flip-Flop

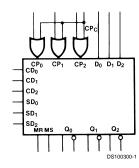
## **General Description**

The 100331 contains three D-type, edge-triggered master/ slave flip-flops with true and complement outputs, a Common Clock (CP<sub>C</sub>), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP<sub>n</sub>), Direct Set (SD<sub>n</sub>) and Direct Clear (CD<sub>n</sub>) inputs. Data enters a master when both CP<sub>n</sub> and CP<sub>C</sub> are LOW and transfers to a slave when CP<sub>n</sub> or CP<sub>C</sub> (or both) go HIGH. The Master Set, Master Reset and individual CD<sub>n</sub> and SD<sub>n</sub> inputs override the Clock inputs. All inputs have 50 k $\Omega$  pull-down resistors.

### **Features**

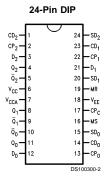
- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9153601

### **Logic Symbol**

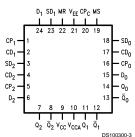


Pin Names	Description
CP <sub>0</sub> -CP <sub>2</sub>	Individual Clock Inputs
CP <sub>C</sub>	Common Clock Input
$D_0-D_2$	Data Inputs
CD <sub>0</sub> -CD <sub>2</sub>	Individual Direct Clear Inputs
SD <sub>n</sub>	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
$Q_0$ - $Q_2$	Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs

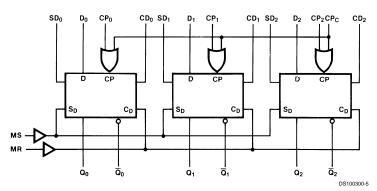
### **Connection Diagrams**



### 24-Pin Quad Cerpak



## **Logic Diagram**



## **Truth Tables**

# **Synchronous Operation** (Each Flip-Flop)

		Outputs			
D <sub>n</sub>	CPn	CPc	MS	Q <sub>n</sub> (t + 1)	
			SD <sub>n</sub>	CDn	
L	~	L	L	L	L
Н	~	L	L	L	н
L	L	~	L	L	L
Н	L		L	L	н
Х	L	L	L	L	Qn(t)
X	Н	X	L	L	Qn(t)
X	X	Н	L	L	Qn(t)

# **Asynchronous Operation** (Each Flip-Flop)

		Outputs			
D <sub>n</sub>	CP <sub>n</sub>	CPc	MS	Q <sub>n</sub> (t + 1)	
			SD <sub>n</sub>	CD <sub>n</sub>	
Х	Х	Х	Н	L	Н
Х	X	Х	L	Н	L
Х	X	X	Н	Н	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
= LOW to HIGH Transition

### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T<sub>STG</sub>)

**Recommended Operating** -65°C to +150°C

-7.0V to +0.5V

Maximum Junction Temperature (T<sub>J</sub>)

+175°C Ceramic

Pin Potential to

Ground Pin  $(V_{EE})$ 

Case Temperature (T<sub>C</sub>)

Military

-55°C to +125°C

 $V_{\text{EE}}$  to +0.5V

-50 mA

≤ 2000V

**Conditions** 

Input Voltage (DC)

(DC Output HIGH)

Output Current

ESD (Note 2)

Supply Voltage (V<sub>EE</sub>)

-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

## **Military Version**

### **DC Electrical Characteristics**

 $V_{EE}$  = -4.2V to -5.7V,  $V_{CC}$  =  $V_{CCA}$  = GND,  $T_{C}$  = -55°C to +125°C

Symbol	Parameter	Min	Max	Units	T <sub>C</sub>	Cond	itions	Notes
V <sub>OH</sub>	Output HIGH Voltage	-1025	-870	mV	0°C to	$V_{IN} = V_{IH}$	Loading with	(Notes 3,
					+125°C	(Max)	50Ω to -2.0V	4, 5)
		-1085	-870	mV	−55°C	or V <sub>IL</sub> (Min)		
V <sub>OL</sub>	Output LOW Voltage	-1830	-1620	mV	0°C to	1		
					+125°C			
		-1830	-1555	mV	−55°C	1		
V <sub>OHC</sub>	Output HIGH Voltage	-1035		mV	0°C to	$V_{IN} = V_{IH}$	Loading with	(Notes 3
					+125°C	(Min)	50Ω to -2.0V	4, 5)
		-1085		mV	−55°C	or V <sub>IL</sub> (Max)		
V <sub>OLC</sub>	Output LOW Voltage		-1610	mV	0°C to	]		
					+125°C			
			-1555	mV	−55°C	1		
V <sub>IH</sub>	Input HIGH Voltage	-1165	-870	mV	−55°C to	Guaranteed HIG	SH Signal	(Notes 3
					+125°C	for all Inputs		4, 5, 6)
V <sub>IL</sub>	Input LOW Voltage	-1830	-1475	mV	−55°C to	Guaranteed LO	W Signal	(Notes 3,
					+125°C	for all Inputs		4, 5, 6)
I <sub>IL</sub>	Input LOW Current	0.50		μA	−55°C to	$V_{EE} = -4.2V$		(Notes 3
					+125°C	$V_{IN} = V_{IL} (Min)$		4, 5)
I <sub>IH</sub>	Input HIGH Current		240	μA	0°C to	V <sub>EE</sub> = -5.7V		(Notes 3
					+125°C	$V_{IN} = V_{IH} (Max)$		4, 5)
			340	μA	−55°C	1		
I <sub>EE</sub>	Power Supply Current	-130	-50	mA	−55°C to	Inputs Open		(Notes 3
					+125°C			4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 5: Sampled tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 6: Guaranteed by applying specified input condition and testing VOH/VOL.

### **AC Electrical Characteristics**

 $V_{\rm EE}$  = -4.2V to -5.7V,  $V_{\rm CC}$  =  $V_{\rm CCA}$  = GND

Symbol	Parameter	T <sub>C</sub> = -55°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f <sub>max</sub>	Toggle Frequency	400		400		400		MHz	Figures 2, 3	(Note 10)
t <sub>PLH</sub>	Propagation Delay	0.50	2.20	0.60	2.00	0.50	2.40	ns		
t <sub>PHL</sub>	CP <sub>C</sub> to Output								Figures 1, 3	
t <sub>PLH</sub>	Propagation Delay	0.50	2.20	0.60	2.00	0.50	2.40	ns		
t <sub>PHL</sub>	CP <sub>n</sub> to Output									
t <sub>PLH</sub>	Propagation Delay	0.50	2.20	0.60	2.00	0.50	2.40		CP <sub>n</sub> , CP <sub>C</sub> = L Figures	(Notes
$t_{PHL}$	CD <sub>n</sub> , SD <sub>n</sub> to Output							ns	1, 4	7, 8,
t <sub>PLH</sub>		0.50	2.40	0.60	2.10	0.50	2.50		CP <sub>n</sub> , CP <sub>C</sub> = H	9)
$t_{PHL}$										
t <sub>PLH</sub>	Propagation Delay	0.70	2.70	0.80	2.60	0.80	2.90		CP <sub>n</sub> , CP <sub>C</sub> = L	
$t_{PHL}$	MS, MR to Output							ns		
t <sub>PLH</sub>		0.70	2.90	0.80	2.80	0.80	3.10		CP <sub>n</sub> , CP <sub>C</sub> = H	
$t_{PHL}$										
t <sub>TLH</sub>	Transition Time	0.20	1.40	0.20	1.40	0.20	1.40	ns	Figures 1, 3, 4	
$t_{THL}$	20% to 80%, 80% to 20%									
t <sub>s</sub>	Setup Time								Figure 5	
	D <sub>n</sub>	1.00		0.80		0.90				(Note
	CD <sub>n</sub> , SD <sub>n</sub> (Release Time)	1.50		1.30		1.60		ns	Figure 4	10)
	MS, MR (Release Time)	2.50		2.30		2.50				
t <sub>h</sub>	Hold Time D <sub>n</sub>	1.50		1.30		1.60		ns	Figure 5	
t <sub>pw</sub> (H)	Pulse Width HIGH									
	CP <sub>n</sub> , CP <sub>C</sub> , CD <sub>n</sub> ,	2.00		2.00		2.00		ns	Figures 3, 4	
	SD <sub>n</sub> , MR, MS									

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25°C. Temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and -55°C Temp., Subgroups A10 and A11.

Note 10: Not tested at +25°C, +125°C and -55°C Temperature (design characterization data).

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### **Test Circuits**

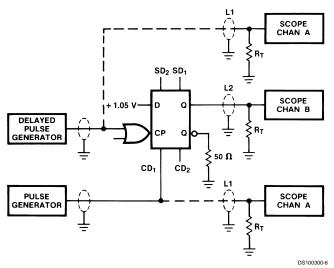
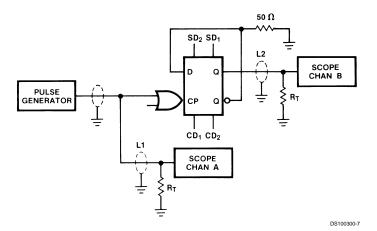


FIGURE 1. AC Test Circuit



#### Notes:

 $V_{CC}$ ,  $V_{CCA}$  = +2V,  $V_{EE}$  = -2.5V L1 and L2 = Equal length 50Ω impedance lines  $R_T$  = 50Ω terminator internal to scope Decoupling 0.1 μF from GND to  $V_{CC}$  and  $V_{EE}$  All unused outputs are loaded with 50Ω to GND  $C_L$  = Fixture and stray capacitance  $\leq$  3 pF

FIGURE 2. Toggle Frequency Test Circuit

## **Switching Waveforms**

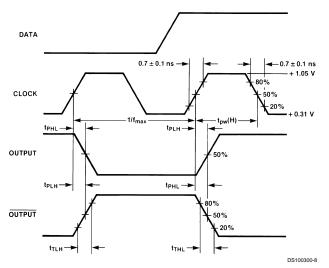


FIGURE 3. Propagation Delay (Clock) and Transition Times

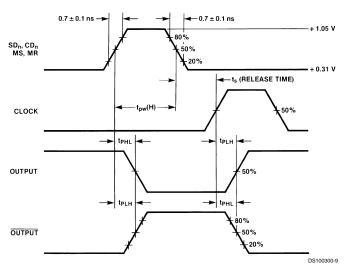


FIGURE 4. Propagation Delay (Resets)

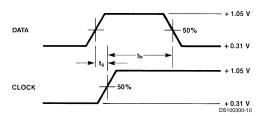
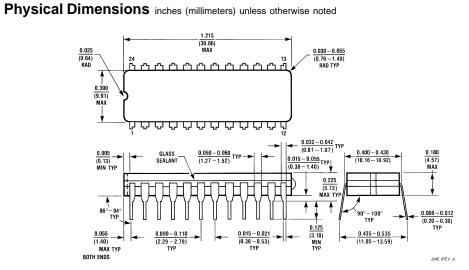
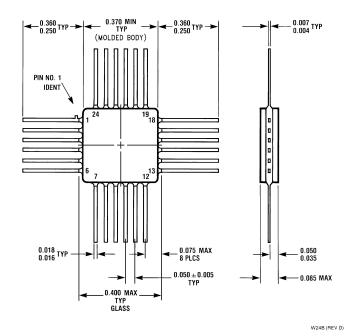


FIGURE 5. Data Setup and Hold Time

Note 11:  $t_s$  is the minimum time before the transition of the clock that information must be present at the data input. Note 12:  $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D) NS Package Number J24E



24-Lead Quad Cerpak (F) NS Package Number W24B

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