OBSOLETE



100325

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100325 Low Power Hex ECL-to-TTL Translator

Check for Samples: 100325

FEATURES

- Pin/function compatible with 100125
- Meets 100125 AC specifications
- 50% power reduction of the 100125
- Differential inputs with built in offset

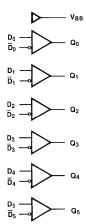
- Standard FAST[®] outputs
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Available to Microcircuit Drawing
 - (SMD) 5962-9153101

DESCRIPTION

The 100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50 kO pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

When used in single-ended operation the apparent input threshold of the true inputs is 20 mV to 40 mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTL} power may be applied in either order.

Logic Diagram



Pin Names	Description		
D ₀ -D ₅	Data Inputs		
$\overline{D}_0 - \overline{D}_5$	Inverting Data Inputs		
Q ₀ -Q ₅	Data Outputs		

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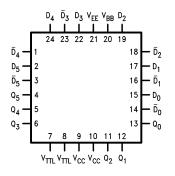
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Connection Diagram

Figure 1. 24-Pin DIP

		\bigcirc		
Q ₅ —	1	-	24	— D ₅
Q4 —	2		23	— D ₅
Q3 —	3		22	$-\bar{D}_4$
ν _{πL} –	4		21	-D4
ν _{πL} –	5		20	— D ₃
v _{cc} –	6		19	— D ₃
v _{cc} –	7		18	- v _{ee}
Q ₂ -	8		17	— v _{BB}
Q ₁ -	9		16	-D2
Q ₀ —	10		15	— D ₂
Ē₀ —	11		14	-D1
D ₀ —	12		13	— D ₁







h	Outputs	
D _n	D _n	Q _n
L	Н	L
Н	L	Н
L	L	L
Н	Н	L
Open	Open	L
V _{EE}	V _{EE}	L
L	V _{BB}	L
Н	V _{BB}	Н
V _{BB}	L	Н
V _{BB}	Н	L

(1) H = HIGH Voltage Level

L = LOW Voltage Level



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings (1)

Above which the useful life may be impaired.	
Storage Temperature (T _{STG})	-65°C to +150°C
Maximum Junction Temperature (T _J)	
Ceramic	+175°C
V _{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
V _{TTL} Pin Potential to Ground Pin	-0.5V to +6.0V
Input Voltage (DC)	V _{EE} to +0.5V
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	-0.5V to V _{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)
ESD ⁽²⁾	=2000V

Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
ESD testing conforms to MIL-STD-883, Method 3015.

Recommended OperatingConditions

Case Temperature (T _C)	
Military	-55°C to +125°C
Supply Voltage (V _{EE})	-5.7V to -4.2V



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Military Version DC Electrical Characteristics

 $V_{EE} = -4.2V$ to -5.7V, $V_{CC} = V_{CCA} = GND$, $T_{C} = -55^{\circ}C$ to +125°C, $C_{L} = 50$ pF, $V_{TTL} = +4.5V$ to +5.5V

Symbol	Parameter	Min	Max	Unit s	т _с	Conditions		Notes
V _{BB}	Output Reference Voltage	-1380	-1260	mV	0°C to +125°C	I _{VBB} = -3 μA, V _{EE} = -4.2V		
						$^{(1)(2)(3)}$ I _{VBB} = -2.1 mA	V _{EE} = -5.7V	-
		-1396	-1260		-55°C	I _{VBB} = -3 mA	† 	
V _{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB})		(1) (2) (3) (4)
V _{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB})		(1) (2) (3) (4)
V _{OH}	Output HIGH Voltage	2.5			0°C to +125°C	L 0.0 m A		(1) (2) (3)
		2.4		mV	-55°C	I _{OH} = -2.0 mA	$V_{IN} = V_{IH (Max)}$ or V _{IL (Min)}	
V _{OL}	Output LOW Voltage		0.5	mV	-55°C to +125°C	I _{OL} = 20 mA		
V _{DIFF}	Input Voltage Differential	150		mV	-55°C to +125°C	Required for Full Output Swing		(1) (2) (3)
V _{CM}	Common Mode Voltage	-2000	-500	mV	-55°C to +125°C			(1) (2) (3) (4)
I _{IH}	Input HIGH Current		350		0°C to +125°C	$V_{IN} = V_{IH (Max)},$		(4) (0) (0)
			500	μA	-55°C			(1) (2) (3)
IIL	Input LOW Current	0.50		μA	-55°C to +125°C			(1) (2) (3)
I _{OS}	Output Short Circuit Current	-150	-60	mA	-55°C to +125°C	V _{OUT} = GND Test One Output at a Time		(1) (2) (3)
I _{CEX}	Output HIGH Leakage Current		250	μA	-55°C to +125°C	V _{OUT} = 5.5V		(1) (2) (3)
I _{EE}	V _{EE} Power Supply Current	-35	-12	mA	-55°C to +125°C			(1) (2) (3)
ITTL	V _{TTL} Power Supply Current		65	mA	-55°C to +125°C	$D_0 - D_5 = V_{BB}$ (1) (2)		(1) (2) (3)

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

(2)

Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8. Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8. (3) (4)

Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

4



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AC Electrical Characteristics

 V_{EE} = -4.2V to -5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T _C =	-55°C	T _C = +25°C		T _C = +125°C		Units	Condition s	Notes
		Min	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagatio n Delay Data to Output	1.50	5.00	1.60	4.70	1.70	5.70	ns	C _L = 50 pF	(1) (2) (3)

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

(2) Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

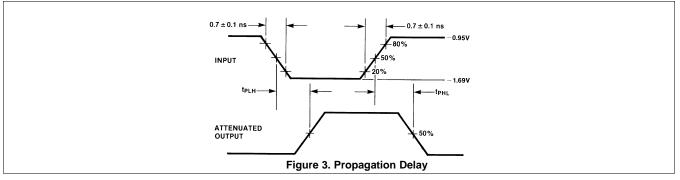
(3) Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and -55°C temperatures, Subgroups A10 and A11.



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Switching Waveform

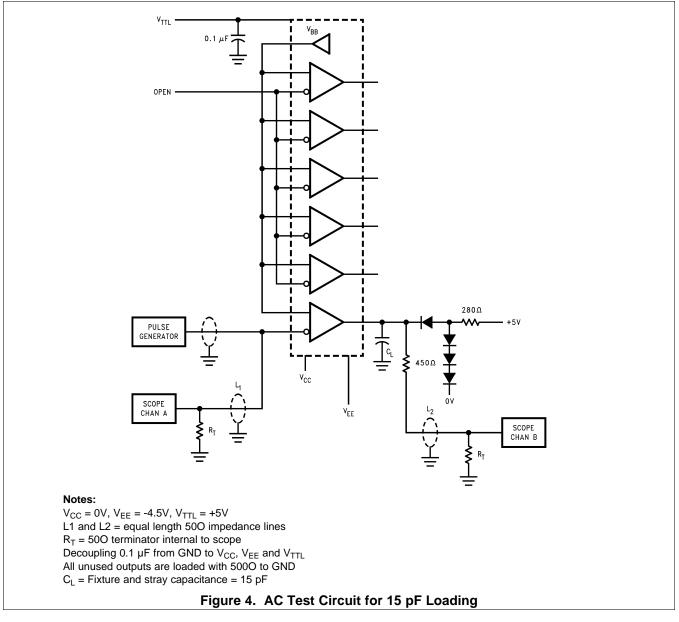




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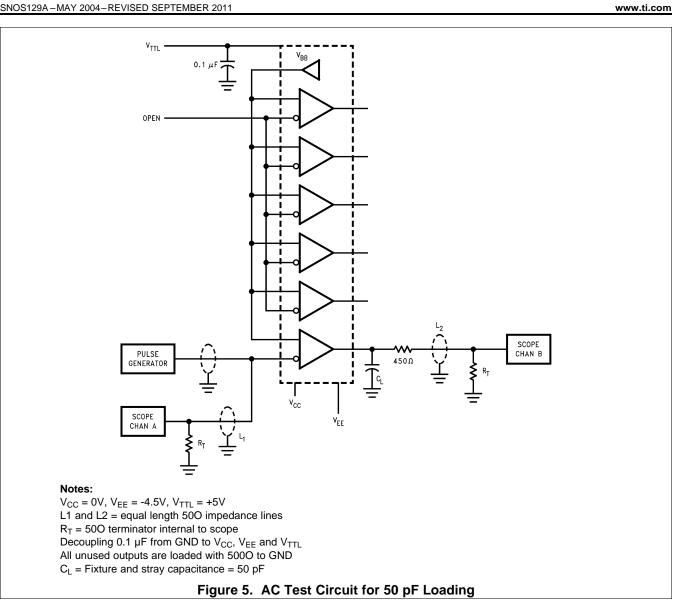
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